CONTROL DATA 8092 TeleProgrammer

PROGRAMMING REFERENCE MANUAL

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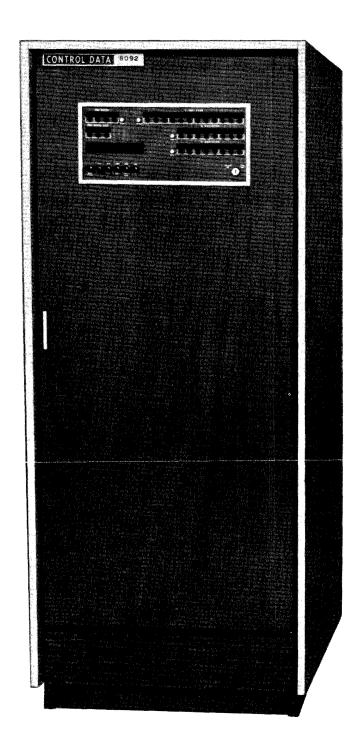
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CHAPTER ONE

PROGRAMMING

GENERAL CHARACTERISTICS

The CONTROL DATA* 8092 TeleProgrammer is a highly flexible and versatile stored program processor specially designed as a high speed buffer memory system for use in a variety of data communication applications.

Among the more important features are the following:

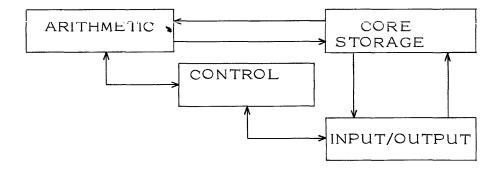
- stored program
- · parallel mode of operation
- 8-bit word length
- 2048 words of core storage 4096 (optional)
- 1 Direct I/O Channel (8 bits)
- 1 Buffer I/O Channel (8 bits)
- · versatile instruction repertoire of 42 instructions
- 3 Auxiliary Tag registers of 4 bits each
- · indirect and direct addressing and modification
- · interrupts
- 12 bit external function address codes
- · 7 internal program registers
- physical size: height, 68 inches; width, 34 inches; depth, 30 inches
- storage reference cycle time of 4 microseconds
- The ability to use the OSAS or OSAS-A assembler for those who have a 160 or 160-A computer.

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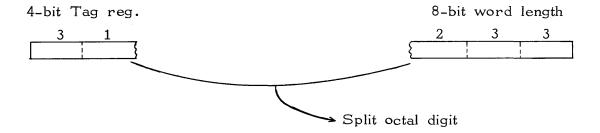
THE CENTRAL PROCESSOR

The TeleProgrammer is a parallel, single address electronic data processor. Operations are controlled by an internally stored program located in sequential addresses. The storage cycle time is 4 microseconds. The basic memory may be expanded from 2048 words to 4096 words. Each internal core word contains 8 bits. Instructions are executed in one to four storage cycle times; with times varying from 4 to 16 microseconds. The average instruction time is approximately 10 microseconds.

The Block Diagram indicates the principal functional divisions

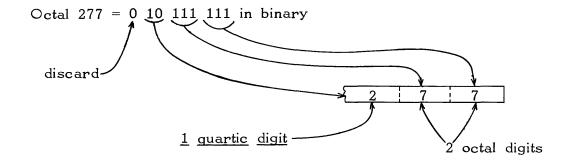


The TeleProgrammer has some unique features for programming. Most of these center around the word length of 8 bits. In order to carry addresses for 4096 registers, 12 bits are required ($2^{12} = 4096$, where highest address is $2^{12} - 1$). To provide for 12 bits, the TeleProgrammer makes use of three 4-bit Tag registers (Tag registers 1, 2, and 3). The carry over from 8 bits to 4 additional bits, in the Tag register, causes a split in the second octal digit from the left. This is indicated below:



In this manual, the 8-bit word length will be represented as two full octal digits and one quartic digit (the leftmost 2 bits). The Tag registers will be generally represented as shown above, with one full octal digit (on the left) and a single bit (0 or 1) on the right. The jagged () ends of the registers indicate the split octal digit.

In addition, this manual will refer to numbers of "three octal digits" being contained in the 8-bit word length. Actually, this is physically impossible, since three octal digits occupy 9 bits and there are only 8 bits in the TeleProgrammer word. However, what is meant here, is that the leftmost bit of the three digit octal number is to be discarded. For example, show the octal number, 277, in a TeleProgrammer word.



This convention of representing the contents of the 8-bit words will be used many times in this manual. Looking at the above 9-bit configuration, one can see that to discard the leftmost bit, it must be zero. This means that the highest quartic digit of the word is 3. This, in turn, indicates the maximum "octal" of three digits which can be expressed in the 8-bit word length; --it is 377. The octal range 000 through 377 is equivalent to 256 registers. Since each Tag register holds 4 bits, there are 16 possible configurations for the 4 bits (0000 through 1111). Thus, 16 times 256 = 4096 total registers available.

WORD FORMAT

People who work with computers are generally acquainted with the term, "octal". It is the number base associated with three bits --which in turn, provides eight possible number states (zero through seven). Since the 8092 TeleProgrammer has an 8-bit word length and partitioning by three bits over the complete word is inefficient; the number base of four with partitioning by two bits is used for the upper two bits of the word. The number base of four, is referred to, in this manual, as QUARTIC. Keep in mind, that only the upper two bits of the word length is expressed in Quartic. The lower six bits are expressed by two octal digits. The upper QUARTIC digit is represented by bits, as shown below:

<u>Bits</u>	The Upper QUARTIC Digit
00	0
01	1
10	2
11	3

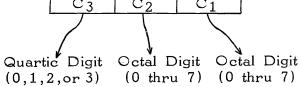
The CONTROL DATA 8092 TeleProgrammer word contains 8 binary digits. These are shown below with the least significant bit (b₀) on the right.

Single Word
Binary Format

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀

Any binary digit above can be represented by any combinations of <u>ones</u> or <u>zeros</u>. Although the 8092 operates in binary, it is more efficient to consider the word format as containing 2 <u>octal</u> and 1 <u>Quartic</u> digits, as shown below:

Single Word Format With Two Octals and One Quartic



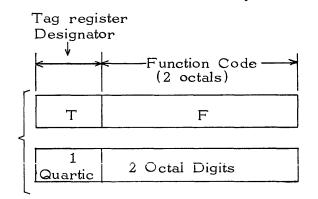
INSTRUCTION WORD FORMAT

The TeleProgrammer operates on a two word instructional set. Most instructions are contained in a set of two sequential storage locations. The first word contains the Function Code, in the lower 2 octal digits, and the Tag register designator, T, in the upper quartic digit. The second word of the instructional set holds: an operand of 2 octals and 1 quartic, or a partial address of 2 octals and 1 quartic. Three modes of operation are possible in the 8092; NO ADDRESS MODE, MEMORY ADDRESS MODE, and INDIRECT ADDRESS MODE. Examples are

shown below:

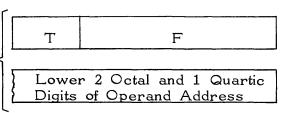
NO ADDRESS MODE

Where T = 0, since there is no Auxiliary Tag register used in this mode. The operand must contain 3 digits in the <u>octal</u> range of 000 thru 377.



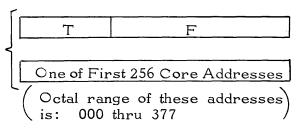
MEMORY ADDRESS MODE

Where T can equal 0, 1, 2, or 3. The lower 8 bits of the operand address appear in the second word and the upper 4 bits of the operand address appear in the Auxiliary Tag register designated by T. If T=0, the address of the operand is fully contained in the second word of the instructional set.



INDIRECT ADDRESS MODE

Where T can equal 0, 1, 2, or 3. At one of the first 256 core locations, given in the second word, is the lower 8 bits of the operand address. The upper 4 bits of this operand address will be found in the Auxiliary Tag register indicated by T.



Examples of the Three Operational Modes

Example 1.

Put the octal number, 277, into the A register.

Solution:

Since no Auxiliary Tag register is involved, T = 0. The octal code for "LOAD A" in this mode is 20; thus F = 20. The octal operand, 277, is placed in the second set as 2 octals (77), and 1 quartic (2).

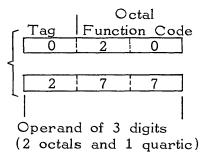
Example 2.

Load the contents of octal address, 3771, into the A register.

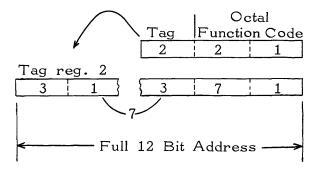
Solution:

The Tag, 2, indicates Auxiliary Tag register 2 holds the upper 2 quartic digits of the address whose lower 8 bits are given in the second instruction word. Note, octal 3771 is contained in the designated Tag register and the second word of the instruction set.





MEMORY ADDRESS MODE



Note: The quartic and 1 bit fit together to form octal, 7, the second digit of the address.

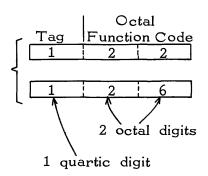
Example 3.

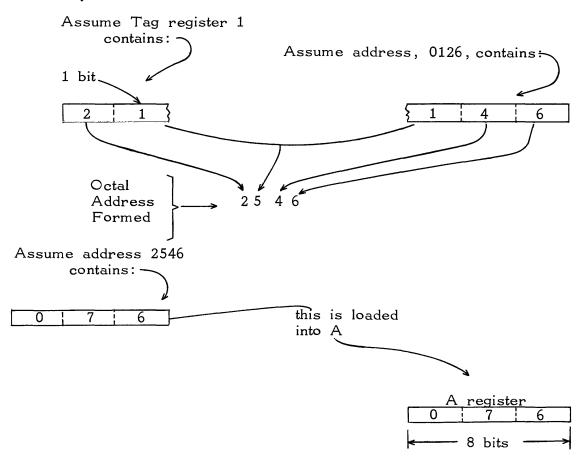
Load the operand whose complete address is in address 0126 and Tag reg. 1.

Solution:

Octal 126 is the address given in the second word. At this address, 0126, the lower 8 bits of the location of the operand are placed. The upper 4 bits of the operand location are placed in Auxiliary Tag register, 1, indicated by the Tag designator of the first word. Continuing this example, assume address 0126 and Tag register 1 contain the quantities shown below, show what finally is loaded into A.

INDIRECT ADDRESS MODE





THE 8092 TeleProgrammer INSTRUCTION REPERTOIRE

Functions	Rel. Code	Octal Code	Cycle Time *	Functions	Rel. Code	Octal Code	Cycle Time
LOADS: Load A (No.) Load A (Mem.) Load A (Ind.) Load Comp. (Mem.) Load Comp. (Ind.) Tag Reg. to A BER to A	LDN LDM LDI LCM LCI TTA BER	20 21 22 25 26 03 06	2 3 4 3 4 1 1	ARITHMETICS: Add (No Adr.) Add (Mem.) Add (Indirect) Subtract (No) Subtract (Mem.) Subtract (Ind.) Replace Add (Mem.) Replace Add 1	ADN ADM ADI SBN SBM SBI RAM RAO	30 31 32 34 35 36 51 55	2 3 4 2 3 4 4 4 4
STORES: Store A (Mem.) Store A (Ind.) A to Tag Reg. A to BER A to BXR	STM STI ATT ABR ABX	41 42 02 04 05	3 4 1 1	LOGICALS: Log. Prod.(No) Log. Prod.(Mem.) Log. Prod.(Ind.) Log. Sum (No) Log. Sum (Mem.) Log. Sum (Ind.)	LPN LPM LPI LSN LSM LSI	10 11 12 14 15 16	2 3 4 2 3 4
JUMPS: If A = 0 If A ≠ 0 If A ≥ 0 If A < 0 Unconditional	ZJP NZP PJP NJP UJP	60 61 62 63 64	2 2 2 2 2	IN-OUT: Input Normal Output Normal Input Buffer Output Buffer Input to A Output No. Adr.	INN OUT IBI IBO INA OTN	72 73 70 71 76 74	** ** 2 2 2 2
SHIFTS: A left 1 bit	SHA	01	1	CONTROLS: Ext. Function Clear Interrupt Clear Buffer Error Stop Halt	EXF CIL CBC ERR HLT	75 13 07 00 77	3 1 1 - 1

^{*} Cycle Times; each cycle = 4 microseconds.

^{**} 3 + 2(X + 1) + terminate time. Where X = No. of words. (Jump cycle times above are 1 less cycle if jump is not made.)

DESCRIPTION AND EXAMPLES OF INSTRUCTIONS

LOAD Instructions

Seven LOAD instruction are available. These are:

LDN - LOAD A (No Address Mode)

LDM - LOAD A (Memory Address Mode)

LDI - LOAD A (Indirect Address Mode)

LCM - LOAD Complement to A (Memory Address Mode)

LCI - LOAD Complement to A (Indirect Address Mode)

TTA - Tag Register Contents to A

BER - Contents of BER Register to A

LDN - (20) - LOAD A (No Address) 2 Cycles

Load the A register with the contents of the second word of the instructional set. Octal numbers 000 through 377 can be entered into A by this instruction.

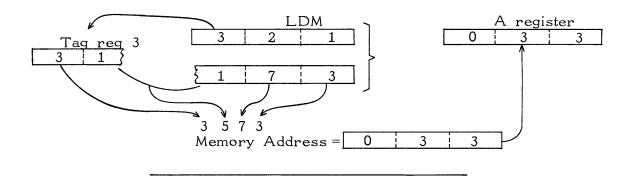
Example: Put the octal number, 177, into A



LDM - (21) - LOAD A (Memory) 3 Cycles

Load the A register with the contents of the memory address whose lower eight bits are given in the second instruction word and whose upper four bits are contained in the designated Auxiliary Tag register.

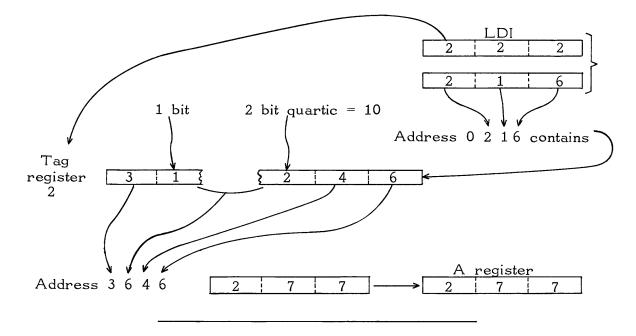
Example: Assume memory address 3573 (in octal) contains the octal quantity, 033. Load this into A.



LDI - (22) - LOAD A (Indirect) 4 Cycles

Load A with the contents of the address whose lower 8 bits are contained in one of the first 256 (decimal) addresses, and whose upper 4 bits are contained in a designated Auxiliary Tag register. The location in the core (one of the first 256 decimal addresses) is given in the second instruction word. The Auxiliary Tag register is indicated in the first word.

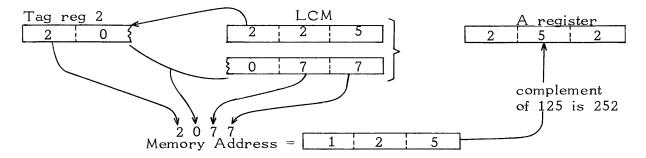
Example: Assume octal address, 3646, contains the octal number, 277. Load this number to A, using the indirect mode via octal address 0216.



LCM - (25) - Load Complement to A (Memory) 3 Cycles

Load the A register with the <u>complement</u> of the contents of the memory address whose lower 8 bits are given in the second instruction word and whose upper 4 bits are contained in the designated Auxiliary Tag register.

Example: Assume memory address 2077 (in octal) contains the octal quantity, 125. Load the complement of this quantity into A.

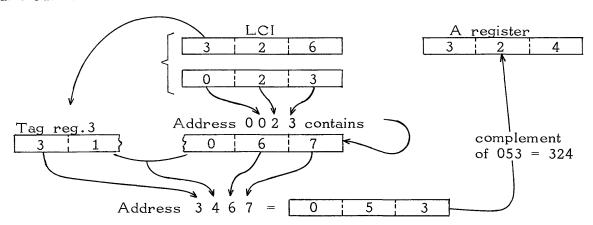


(Note: quartic complements are "three's complement". Thus, the complement of the quartic digit, 1, above is 2; whereas, the complements of the octal digits 2 and 5 are respectively 5 and 2.)

LCI - (26) - Load Complement to A (Indirect) 4 Cycles

Load A with the complement of the contents of the address whose lower 8 bits are contained in one of the first 256 (decimal) addresses and whose upper 4 bits are contained in the designated Auxiliary Tag register. The location in the core (one of the first 256 decimal addresses) is given in the second instruction word. The Auxiliary Tag register is indicated in the first word.

Example: Assume octal address 3467 contains the octal number, 053. Load the complement of this number into A, using the indirect mode and via octal location 0023.

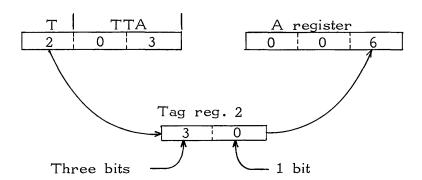


Note: The 1 bit of Tag register 3 and the quartic digit at address 023, form the bits, 100, which gives the octal digit, 4. Also note, the complement of the quartic digit, 0, at address 3467 is equal to 3; whereas, the complements of the octal digits 5 and 3 are respectively equal to 2 and 4.

TTA - (03) - Tag Register to A 1 Cycle

Load the contents of the designated Auxiliary Tag register into the A register. Pack zero's in upper 4 bits.

Example: Load contents of Tag register, 2, into A.

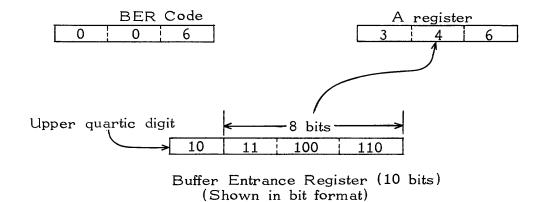


Note: The four bits of the Tag register are: 0110. When packed to the right of A, they give the following: $00\ 000\ 110 = 006$.

BER - (06) - Buffer Entrance Register to A 1 Cycle

Load the A register with the lower 8 bits of the Buffer Entrance register.

Example: Load Buffer Entrance register into A



Note: On this instruction, the lower 8 bits (1 quartic and 2 octals) are transferred into the A register. The upper 2 bits (1 quartic digit) are not transferred. On the reverse transfer (A to BER), the right 2 bits of Tag register 3 are sent to the upper 2 bit locations of BER. This is explained in detail in the ABR instruction.

The above concept may be clearer to the reader if its is remembered that twelve bits, rather than eight bits, are required to cover the whole possible address range of 4096 registers. As a consequence, it must be possible to perform buffer operations covering the complete address range. To accomplish this, the BER (of 10 bits) uses the 8 bits of the instruction operand, 2 bits from Tag register 3 (the rightmost 2 bits). By referencing the leftmost 2 bits of Tag register 3, the full 12 bits are made available.

STORE Instructions

Five STORE instructions are available; these are:

STM - STORE A (Memory Address Mode)
STI - STORE A (Indirect Address Mode)

ATT - A to Tag Register

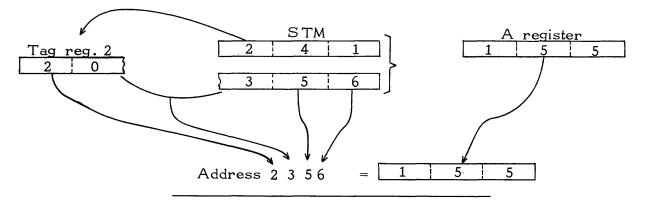
ABR - A to Buffer Entrance Register

ABX - A to Buffer Exit Register

STM - (41) - STORE A (Memory Mode) 3 Cycles

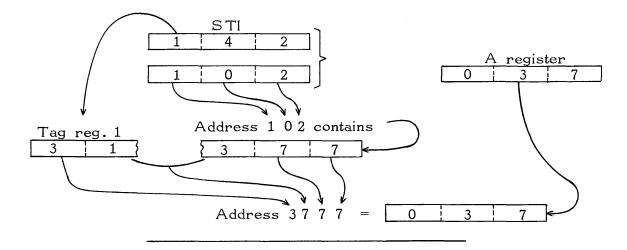
Store the contents of the A register into the location whose address is equivalent to the combined contents of the designated Tag register and the second word of the instruction set.

Example: Assume A contains the octal number, 155. Store this number at octal address, 2356.



STI - (42) - STORE A (Indirect Mode) 4 Cycles

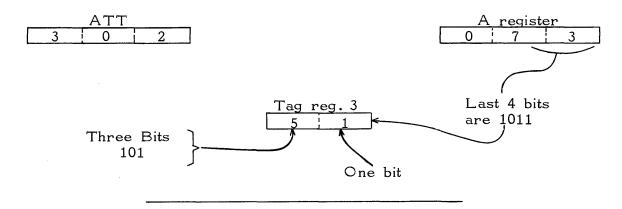
Store the contents of the A register into the location whose address is equivalent to the combined contents of the designated Tag register and the contents of one of the first 256 decimal core registers. The exact location of one of these 256 registers is given, through its address, in the second instruction word. Example: Assume the A register contains the octal number, 037. Store this number in octal address, 3777, by using octal location 0102, and the indirect mode.



ATT - (02) - A to Tag Register 1 Cycle

Transfer the lower 4 bits (2 quartic digits) of the A register into the designated Auxiliary Tag register.

Example: Assume the A register contains the octal number, 073. Store the A register at Auxiliary Tag register, 3.



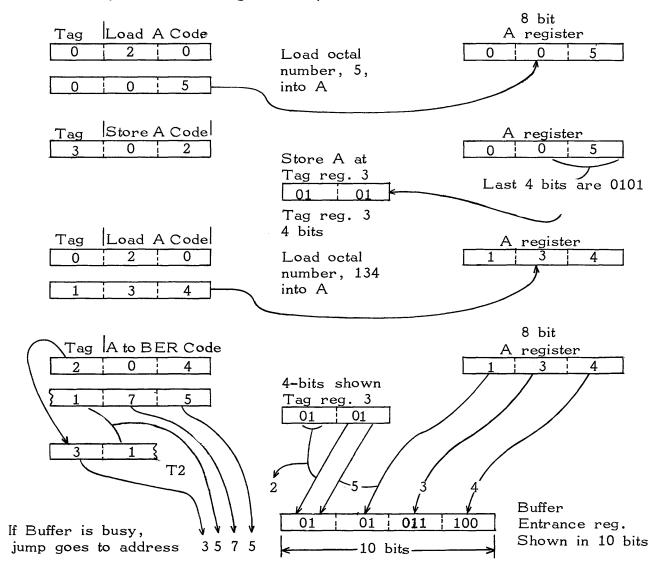
ABR - (04) - A to Buffer Entrance Register 1 Cycle

Transfer the contents of A to the lower 8 bit positions of the Buffer Entrance register. The rightmost 2 bits of Tag register 3 become the 9th and 10th bits

of the Buffer Entrance Register (BER); the upper two bits of Tag register 3 are referenced for bits 11 and 12 of BER. If the buffer is busy, a jump occurs to the combined address contained in the second word of the instruction set and the designated Tag register. If the buffer is not busy, control goes to the next instructional set.

Example: Assume one wants to effectively enter a starting octal address of 2534 into the Buffer Entrance register. Shown are the program steps involved.

To effectively enter a starting address, 2534 into BER



Since BER is a 10-bit register, there is not room for the full 12-bit address. The upper 2 bits (1 quartic) are obtained by <u>referencing</u> the left 2 bits of Tag register 3. In the above example, the left 2 bits of Tag register 3 and the leftmost bit of BER give the octal digit, 2.

ABX - (05) - A to Buffer Exit Register 1 Cycle

Transfer the contents of A to the lower 8 bits of the Buffer Exit register (BXR). The right <u>quartic</u> digit (2 bits) of Tag register 3 fills the 2 leftmost bits of BXR. The left <u>quartic</u> digit of Tag register 3 is <u>referenced</u> by the TeleProgrammer to determine the leftmost 2 bits of the address.

If the buffer is busy a jump occurs to the combined address contained in the designated Tag register of the first word and the contents of the second word of the instruction set. If not busy, control continues to the next instruction set in sequence.

Example: Show a program which places octal address, 3520 into BXR; if the buffer is busy, wait until it is not busy.

Location of Instruction	Instructions	Explanation of Action which Occurs			
3420 3421	020 007	Load A with the octal number, 007.	007 → A		
3422	302	Store lower 4 bits of A at Tag register, 3.	Bits, 0111, go to Tag reg.3		
3423 3424	020 120	Load A with the octal number, 120.	120 → A		
3425 3426	305 025	A goes to bits 1 thru 8 of BXR, right quartic (3) of Tag reg. 3 goes to bits 9 and 10 of BXR. Left quartic digit of Tag reg. 3 is referenced for upper 2 bits of address.			
If buffer is busy, jump goes to combined address of designated Tag. reg. and contents of second word. In this example, jump goes to 3425. Tag reg. 3 (in bits) O 1 11 1 2 Upper quartic is referenced for leftmost part of address. This combined with leftmost bit of BXR gives octal digit, 3.					

JUMP INSTRUCTION

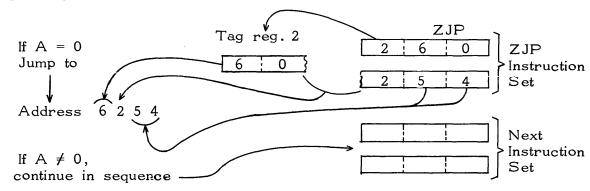
Five JUMP instructions are available, they are:

ZJP - JUMP, if contents of A = 0
NZP - JUMP, if contents of A ≠ 0
PJP - JUMP, if contents of A ≥ 0 (positive)
NJP - JUMP, if contents of A < 0 (negative)
UJP - Unconditional JUMP

ZJP - (60) - Zero JUMP 2 Cycles if jump is made; otherwise, 1.

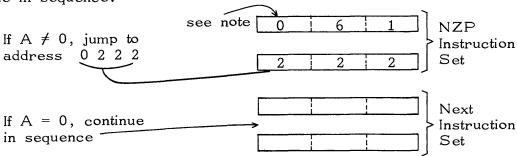
If the contents of A equals zero, jump to the <u>combined</u> address contained in the designated Tag register and the second word of the instruction set. If the contents of A are not zero, continue in sequence with next <u>set</u> of instructions.

Example: Test A for zero, and jump to octal address, 6254, if A is zero; otherwise continue.



NZP - (61) - Not Zero JUMP 2 Cycles if jump is made; otherwise, 1. If contents of A are not zero, jump to the combined address contained in the designated Tag register and the second word of the instruction set. If the contents of A are zero, continue in sequence with the next set of instructions.

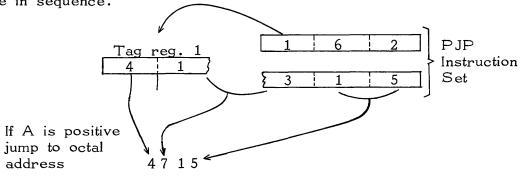
Example: Test A, and if not zero, jump to octal address, 0222. If zero, continue in sequence.

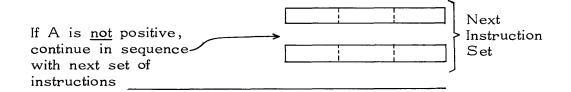


Note: Since the complete jump address can be expressed in 8 bits, no Tag register is required. Thus, the Tag designation = 0, in the first instruction word.

<u>PJP - (62) - Positive JUMP</u> 2 Cycles if jump is made; otherwise, 1. If the contents of A are positive (equal or greater than zero), jump to the combined address contained in the designated Tag register and the second word of the instruction set. If the contents of A are not positive, continue in sequence. (If leftmost bit = 0, contents of A are positive.)

Example: Test A, and if positive, jump to octal address 4715. Otherwise, continue in sequence.

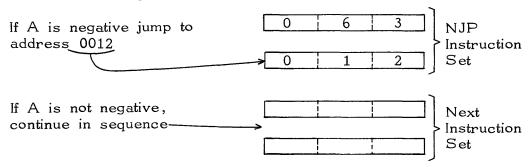




NJP - (63) - Negative JUMP 2 Cycles if jump is made; otherwise, 1.

If the contents of A are negative, jump to the combined address contained in the designated Tag register and the second word of the instruction set. If the contents of A are not negative, continue in sequence with the next set of instructions.

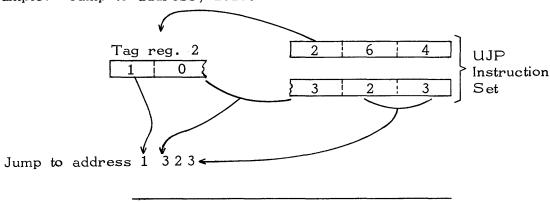
Example: Test A, and if negative, jump to octal address, 0012. If not negative, continue in sequence.



Since significant portion of the address can be contained in 8 bits, no Tag register is required and thus Tag designation of first instruction word is zero.

<u>UJP - (64) - Unconditional JUMP</u> 2 Cycles if jump is made; otherwise, 1. Jump to the <u>combined</u> address contained in the designated Tag register and the second word of the instruction set.

Example: Jump to address, 1323.



SHIFT INSTRUCTION

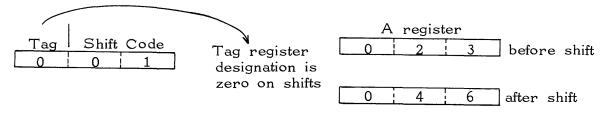
One shift instruction is available:

SHA = SHIFT A LEFT ONE BIT

SHA - (01) - Shift A Left 1 1 Cycle

Shift the contents of A left--end around--1 bit position. Bits coming off the left end of the A register enter the lowest bit position on the right end of the register.

Example: Assume A contains the octal number 023. Multiply the contents of A by 2, using the shift instruction.



Note: One shift instruction is required to shift A one place (1 bit) to the left. Each left shift is equivalent to one multiplication by 2. To shift 5 bits left, it is necessary to give 5 shift instructions, or loop through the single shift instruction 5 times.

ARITHMETIC INSTRUCTIONS

There are eight Arithmetic instructions: three adds, three subtracts, and two replace adds. These are:

ADN - ADD (No Address)

ADM - ADD (Memory Address)
ADI - ADD (Indirect Address)

SBM - SUBTRACT (No Address)

SBM - SUBTRACT (Memory Address)
SBI - SUBTRACT (Indirect Address)

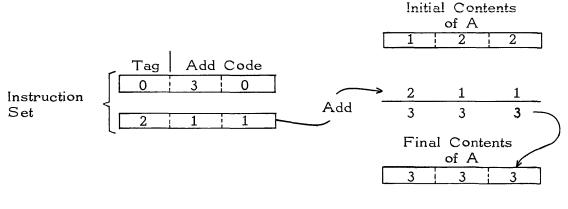
RAM - REPLACE ADD (Memory Address)

RAO - REPLACE ADD ONE (Memory Address)

ADN - (30) - ADD (No Address) 2 Cycles

Add to the A register the 8 bit number given in the second word of the instruction set. The sum is left in A.

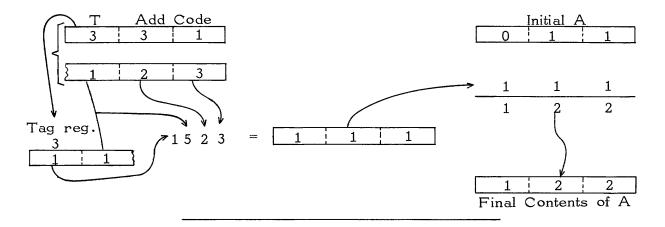
Example: Assume A contains the octal number, 122. Add the octal number, 211, to A.



ADM - (31) - ADD (Memory Address) 3 Cycles

Add to A the contents of the combined address given in the designated Tag register and the second word of the instruction set.

Example: Assume A contains the octal, 011. Add the contents of address 1523 to A. (Assume contents of address 1523 are 111.)



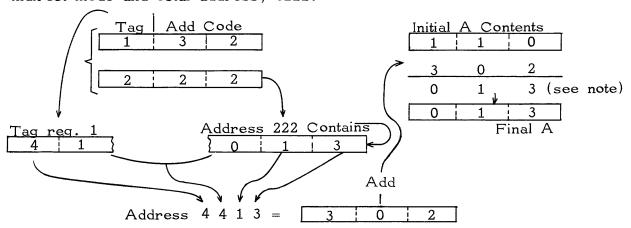
ADI - (32) - ADD (Indirect Address) 4 Cycles

Add to A the contents of the combined address contained in the designated

Tag register and one of the first 256 decimal locations indicated in the second

word of the instruction set.

Example: Assume A contains octal number, 110. Assume octal address, 4413 contains 302. Add the contents of address 4413 to A, by using the indirect mode and octal address, 0222.

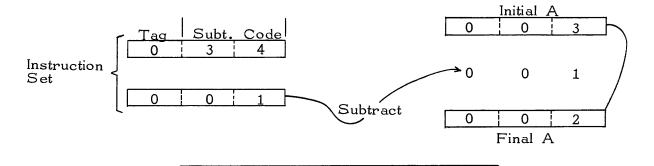


Note: The addition of 1 and 3 in the rightmost quartic digits overflows the register and the carry over (1) is added to the rightmost digit.

SBN - (34) - SUBTRACT (No Address) 2 Cycles

Subtract from the A register, the number contained in the second word of the instruction set. The difference is left in A register.

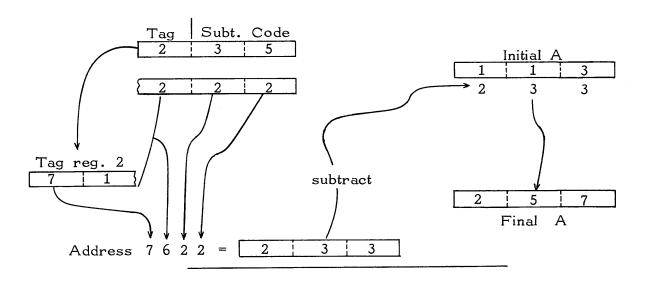
Example: Assume A contains 003. Subtract 001.



SBM - (35) - SUBTRACT (Memory Address) 3 Cycles

Subtract from the contents of A, the contents of the combined address contained in the designated Tag register and the second word of the instruction set.

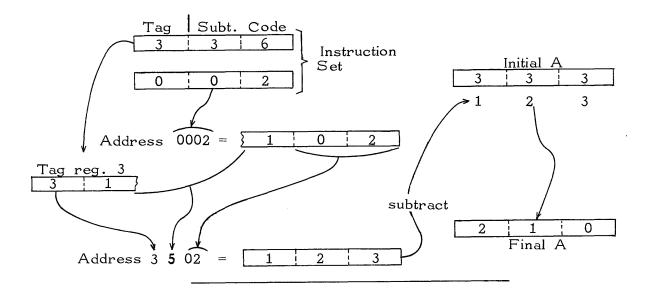
Example: Assume A contains the octal, 113. Assume address, 7622 contains 233. Subtract the contents of address 7622 from A.



SBI - (36) - SUBTRACT (Indirect Address) 4 Cycles

Subtract from the contents of A, the contents of the combined address contained in the designated Tag register and the location of one of the first 256 decimal registers, indicated by the second word of the instruction set.

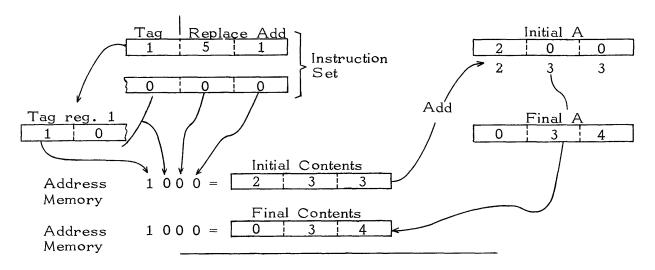
Example: Assume A contains the octal, 333. Assume address 3502 contains the octal number, 123. Reduce A by the contents of address 3502, using indirect mode and octal address, 0002.



RAM - (51) - REPLACE ADD (Memory Address) 4 Cycles

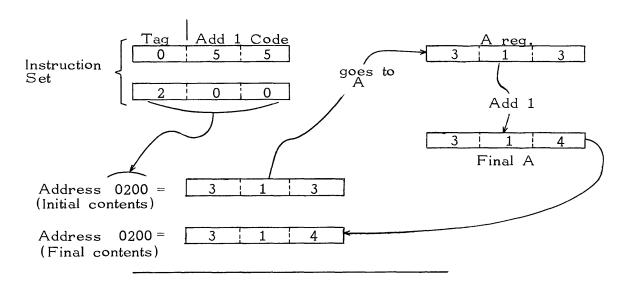
Add the contents of the A register to the contents of the memory address formed by the contents of the designated Tag register and the second word of the instruction set. The sum thus formed, remains in A, and replaces the initial contents of the memory address.

Example: Assume A contains the octal number, 200. Assume address 1000 contains the octal number, 233. Increase the contents of address 1000 by the contents of A.



RAO - (55) - REPLACE ADD ONE 4 Cycles

Add 1 to the contents of the memory address indicated by the combined contents of the designated Tag register and the second word of the instruction set. This sum is performed in A and remains in A at the end of the instruction. Example: Add 1 to the contents of memory address, 0200.



LOGICAL INSTRUCTIONS

There are six Logical instructions: three of which are Logical products; three are Logical sums. These are:

LPN - LOGICAL PRODUCT (No Address)
LPM - LOGICAL PRODUCT (Memory Address)
LPI - LOGICAL PRODUCT (Indirect Address)

LSN - LOGICAL SUM (No Address)
LSM - LOGICAL SUM (Memory Address)
LSI - LOGICAL SUM (Indirect Address)

Logical Product is defined as a "by by bit" multiply which observes the following rules:

1 times 0 = 0 0 times 0 = 0 0 times 1 = 0 1 times 1 = 1

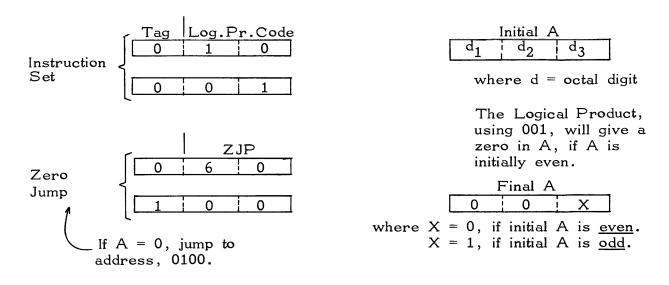
Logical Sum is a "by by bit" sum without "carries" which observe the following rules:

 $\begin{array}{rclr} 1 & + & 0 & = & 1 \\ 0 & + & 1 & = & 1 \\ 0 & + & 0 & = & 0 \\ 1 & + & 1 & = & 0 \end{array}$

LPN - (10) - LOGICAL PRODUCT (No Address) 2 Cycles

Form in A the Logical Product of the contents of A and the contents of the second word of the instruction set.

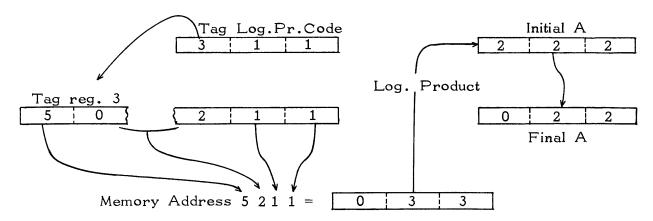
Example: Test A for "even". If even, jump to octal address, 0100.



LPM - (11) - LOGICAL PRODUCT (Memory Address) 3 Cycles

Form in A, the Logical Product of the contents of A and the contents of the memory location whose address is the combined contents of the designated Tag register, and the second word of the instruction set. The initial contents of the memory location remains unchanged.

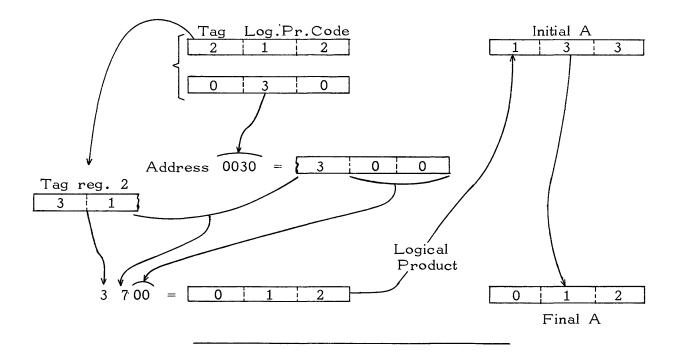
Example: Assume A contains the octal, 222. Assume memory address, 5211, contains 033. Form the Logical Product in A.



LPI - (12) - LOGICAL PRODUCT (Indirect Address) 4 Cycles

Form in A the Logical Product of the contents of A and the contents of the memory location whose address is the combined contents of the designated Tag register and the contents of one of the first 256 decimal locations. The address of this decimal location is given in the second word of the instruction set. The initial contents of the memory location remain unchanged.

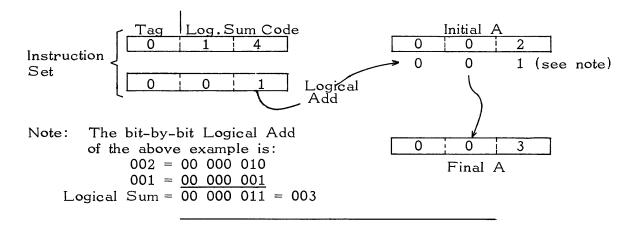
Example: Use the indirect mode to form the Logical Product of A and memory location 3700. Use octal location, 0030 in the process. Assume initial contents of A and location 3700 are respectively: 133 and 012.



LSN - (14) - LOGICAL SUM (No Address) 2 Cycles

Form in A the Logical Sum of the contents of A and the second word of the instruction set.

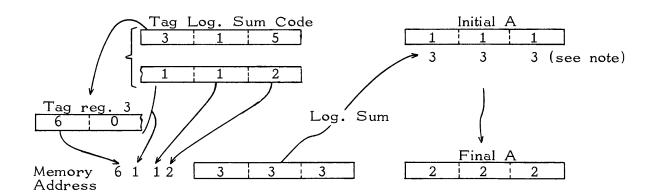
Example: Assume A contains octal number, 002. Set A to 003.



LSM - (15) - LOGICAL SUM (Memory Address) 3 Cycles

Form in A the Logical Sum of the contents of A and the contents of the memory location whose combined address is given in the designated Tag register and the second word of the instruction set.

Example: Assume A contains octal number, 111. Form in A the Logical Sum of the contents of A and the contents of memory location, 6112. Assume this location contains 333.

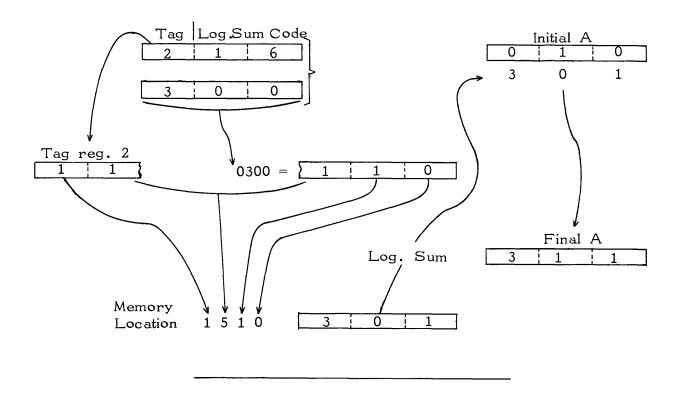


Note: The Logical Sum performed above, is shown below in bit form.

LSI - (16) - LOGICAL SUM (Indirect Address) 4 Cycles

Form in A the Logical Sum of the contents of A and the contents of the memory location whose address is the combined contents of the designated Tag register and one of the first 256 (decimal) locations. The location of one of these 256 locations is given in the second word of the instruction set.

Example: Assume A contains 010. Assume memory location, 1510, contains 301. Using the indirect mode, and location 0300, form in A the Logical Sum of the contents of A and the contents of address 1510.



INPUT-OUTPUT INSTRUCTIONS

There are six instructions directly related to input-output functions. These are:

INN - INPUT NORMAL
OUT - OUTPUT NORMAL

IBI - INITIATE BUFFER INPUT IBO - INITIATE BUFFER OUTPUT

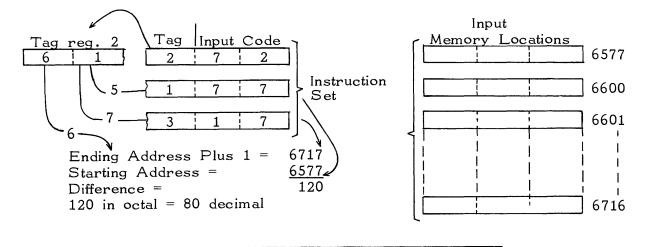
INA - INPUT TO A

OTN - OUTPUT NO ADDRESS

INN - (72) - INPUT NORMAL (see p. 9 for timing)

Input a number of words to memory starting at the memory address contained in the designated Tag register and the second word of the instruction. The ending address plus 1, is contained in a third word immediately following the second word. Thus, this instruction set is composed of three words. (The Tag register designation indicated in the first word is automatically assigned as the Tag register designation for the ending address plus 1, in the third word.)

Example: Input 80 words to memory starting at octal address, 6577.

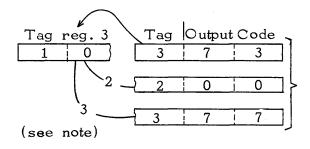


OUT - (73) - OUTPUT NORMAL

Output a number of words from memory starting at the memory address contained in the designated Tag register and the second word of the instruction set.

The ending address plus 1, is contained in a third word immediately following. Thus, this instruction set is composed of three words. (The Tag register designation, indicated in the first word is automatically assigned as the Tag register designation for the ending address plus 1, in the third word.)

Example: Output 300 (decimal) words from memory, starting at octal



address, 1200.

First 127 (decimal) words are outputed from octal addresses shown:

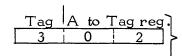
Ending Address Plus 1 = 1377

Starting Address = 1200

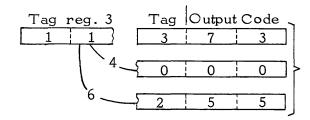
Number of Words = 177 = 127

_	Tag	Load	A Code
	0	2	0
			}
	0	0	3

Load A with 003.



Change Tag register, 3, by storing A at Tag register 3. Tag register 3 now contains 0011 (in bits).



Next 173 (decimal) words are outputed from octal addresses shown:

Ending Address Plus 1 = 1655

Starting Address = $\frac{1400}{255}$ Number of Words = $\frac{1400}{255}$

127 + 173 = total 300 words

NOTE:

The "ending address plus 1" of 1377 above, resulted in a "gap"--that is, no output came from this register. The reason is that quartic address, 1377, falls at a "boundary address" as far as the addressing logic of the Tele-Programmer is concerned. "Boundary addresses" are those, which when incremented by 1, cause a change to occur in any one of the 4 leftmost address bits. This in turn, requires a change in the Tag register (as above). There are 16 such "boundary addresses" in the whole 4096 registers. This condition is not serious due to the following alternatives:

- (a) If output follows input or vice versa such "gaps" would have existed in the identical places anyway, and thus are of no consequence.
- (b) If one wishes, he can fill the gap location by loading one word into A and storing at the gap address.
- (c) By effective memory allocation, boundary addresses can often be entirely avoided.
- (d) Buffered operations do not have this situation.

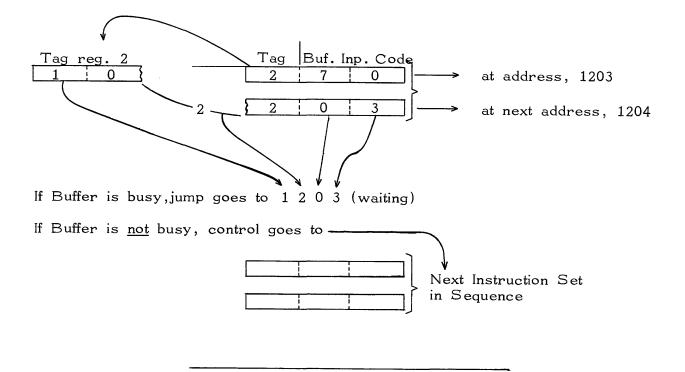
The previous example was given to indicate that a change in address which changes <u>any one</u> of the 4 leftmost bits of the 12-bit address, requires a corresponding change in the contents of the Tag register. It should be apparent, that the maximum transfer <u>without changing the Tag register</u> is 256 (decimal words.

IBI - (70) - INITIATE BUFFER INPUT

Before using this instruction, the starting address of the buffer transfer is sent to BER, and the ending address plus 1 is sent to BXR (see these instructions).

This instruction initiates the input buffer cycle. If the buffer channel is not busy, control goes to the next instruction following the second word of the instruction set. If the buffer channel is busy, a jump occurs to the memory location whose combined address is contained in the designated Tag register and the second word of the instruction set.

Example: Initiate buffer input, and if busy wait until not busy. Assume the instruction is given at the location whose octal address is, 1203.

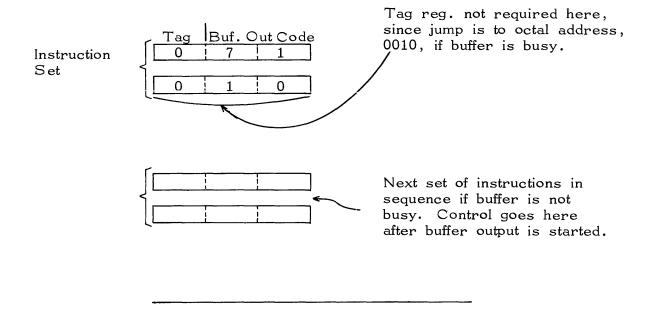


IBO - (71) - INITIATE BUFFER OUTPUT

Before using this instruction, the starting address of the buffer transfer must be sent to BER, and the ending address plus 1 must be sent to BXR (see these instructions).

This instruction initiates the output buffer cycle. If the buffer channel is busy, a jump occurs to the combined memory address given in the designated Tag register and the second word of the instruction set. If the buffer channel is not busy, control goes to the next sequential instruction following the instruction set.

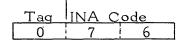
Example: Initiate buffer output and if busy jump to octal address 0010.



INA - (76) - INPUT TO A

This instruction <u>inputs</u> <u>one</u> word from a previously selected input device to the A register.

Example: Assume a previous instruction (see EXF) has selected the paper tape reader for input. Input one frame (one word) to A.

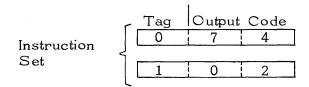


Note: This is a <u>single</u> word instruction, and the Tag register designation is <u>always</u> zero.

OTN - (74) - OUTPUT NO ADDRESS

This instruction outputs one word. This word is the second word of the instruction set.

Example: Assume a previous instruction has selected the Printer. Output the number 0102.



Note: The Tag register designation is always zero in this instruction.

CONTROL INSTRUCTIONS

Five Control instructions are available:

EXF - EXTERNAL FUNCTION

CIL - CLEAR INTERRUPT LOCKOUT

CBC - CLEAR BUFFER CONTROLS

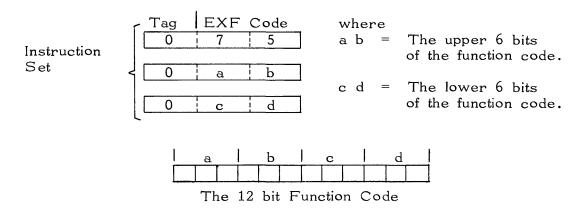
ERR - ERROR STOP

HLT - HALT

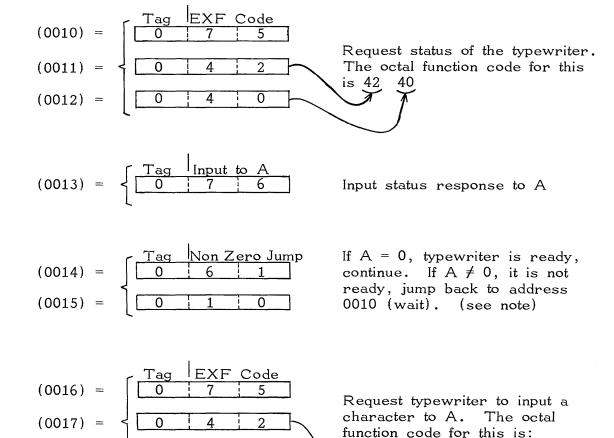
EXF - (75) - EXTERNAL FUNCTION

This instruction is used to <u>select</u> an external input or output device to communicate with the TeleProgrammer. The select function is accomplished by sending out on the output lines a 12-bit "function code". Each external device is capable of recognizing and interpreting only its own unique code. Thus, the programmer by selecting different external function codes can use this same instruction to select all external devices.

The 12-bit function code is contained in the <u>second</u> and <u>third</u> words of the three words which make up this instruction set. The format of the three words are best described by the following:



Example: Request the status of the typewriter (ready or not ready), if busy, wait; request typewriter input; and input to A.



$$(0021) = \begin{cases} Tag & Input to A \\ \hline 0 & 7 & 6 \end{cases}$$
 Input the character to A

(0020) =

Note: In the jump back to address 0010 above, no Tag register is required since the octal address is one whose significant bits can be expressed in 8 bits.

CIL - (13) - CLEAR INTERRUPT LOCKOUT

This instruction clears the interrupt lockout flip flop (FF). This instruction must be programmed at the end of every routine which is initiated by the interrupt. This instruction returns control to the main program.

Example: Assume an interrupt has occurred and a routine entered. At the end of this routine show the instruction required to clear the Interrupt Lockout and return control to the Main Program.

Tag	CIL	Code	
1	1	3	

Note: In this instruction, the Tag designation becomes a part of the function code itself. It can only be 0 or 1. Thus, to return to main program after clearing interrupt lockout, the Tag designation must be 1. If zero, control continues in sequence.

CBC - (07) - CLEAR BUFFER CONTROLS

This instruction has the effect of sending a zero to buffer control and thus putting that device in a "ready state". If this instruction is used <u>during</u> a buffer operation, it will stop the buffer.

Example: Clear buffer control.

Tag	CBC	Code	
0	0	7	

A Tag register designation is ignored in this single word instruction.

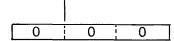
Two STOPS are available; these are:

ERR = ERROR STOP HLT = HALT STOP

ERR - (000) - ERROR STOP

This is an illegal instruction -- as such, it can be used as an Error Stop.

Example: Use the Error Stop instruction.

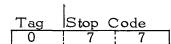


Error Stop

HLT - (77) - PROGRAM STOP

This instruction is used to bring the program to a halt.

Example: Use the STOP instruction.



Program Stop

CHAPTER TWO OPERATION

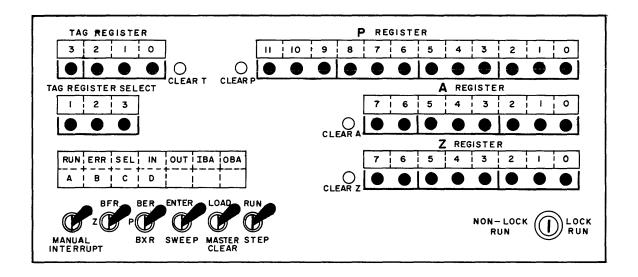


Figure 2-1 8092 Operator's Panel

TeleProgrammer OPERATOR's CONSOLE

The 8092 TeleProgrammer Operator's Panel consists of several displays and switches necessary for the operation of the TeleProgrammer. The panel (see figure 2-1) contains six display windows, six switches, and a lock switch. Four of the display windows can display in binary the contents of nine 8092 registers. Buttons beneath these displays clear and enter data into the P, A, Z, and Tag registers (the only registers into which data may be entered or cleared). A fifth window contains information as to which Tag register has been selected. The sixth window contains the operating lights which indicate the status of operation

of the TeleProgrammer. At the bottom of the panel is located all the operating and mode switches. The operation of these switches is explained below:

SWITCHES

Manual Interrupt

-Momentary depression causes the Teleprogrammer to enter an interrupt routine to determine the nature of the interrupt.

BFR,Z

-This 3-position switch chooses the register that is to be displayed in the 8-bit Z register display.

<u>Up</u> - Displays the last word processed during the last buffer operation (BFR register).

<u>Center</u> - Shows the current contents of the Z register (Z register).

<u>Down</u> - Not assigned.

BER, P, BXR

-This 3-position switch chooses the register to be displayed in the 12-bit P register display.

<u>Up</u> - Displays the address of the last word transferred out, the next word to be transferred in on the buffer channel (BER register).

<u>Center</u> - Displays the address of the current instruction (P register).

<u>Down</u> - Displays the LWA + 1 of the last buffer operation (BXR register).

ENTER/SWEEP

-Sweep is used to display the contents of core storage locations. Enter is used for entering information into core storage from the console.

LOAD/MASTER CLEAR

- LOAD position allows specially prepared paper tapes to be read into storage by the paper tape reader.

Master CLEAR performs a TeleProgrammer master clear which

- a. Clears the registers
- b. Clears the control flip flops
- c. Clears all waiting interrupts and removes interrupt lockout.

Note: The master clear does not alter core storage.

RUN/STEP

<u>Up</u> - In RUN position a program is executed at high speed starting at the location specified by the P register.

Center - Center position stops the computer program. If the switch is in RUN and an ERR or HLT instruction is executed, the switch must be returned to neutral and then placed in RUN to continue computation.

Down - In STEP position, one storage cycle of an instruction is executed each time the switch is set; a program may be executed one instruction at a time for debugging.

NON-RUN LOCK RUN LOCK In the Lock position all other switches are disabled and the TeleProgrammer is locked in the RUN position.

In the non-lock position, the console switches are enabled and the TeleProgrammer programs can be operated and modified from the console.

DISPLAYS

Z REGISTER

-This display known as the Z register group displays the Z and BFR registers in accordance with the setting of the BFR, Z switch.

A Register

-Displays the current contents of the A register.

P Register

-This display known as the P register group displays the BER, P, and BXR registers in accordance with the setting of the BER, P, BXR switch.

TAG REGISTER

-This display indicates the Tag register currently being referenced by an instruction. The contents of any Tag register may be displayed by depressing one of the buttons directly below the select indicators. Depressing one of the select buttons also enables the Tag registers to be manually set or cleared.

STATUS INDICATORS

<u>RUN</u>

-Indicates that the TeleProgrammer is in RUN status. This does not necessarily indicate that instructions are being executed.
-Indicates that a timing fault has occurred.
-Displayed each time an EXF instruction

is executed; remains until selection is

completed. A constant display of SEL

with no apparent input/output action usually

indicates the TeleProgrammer has attempted

ERR

SEL

an illegal selection.

<u>IN</u>

-Displayed during all normal input operations. A constant display of IN with no apparent input action usually indicates that input was attempted without proper unit selection. IN is also displayed when the TeleProgrammer is waiting for an external device to supply data.

Displayed during all normal output operations. A constant display of OUT with no apparent output action usually indicates that output was attempted without proper unit selection.

Displayed during all buffer input operations.

Displayed during all buffer output operations.

Indicates which storage reference cycle will

be executed at the next operation of the

Run/Step switch. When a master clear

is performed, D is displayed indicating

that the next operation to be executed,

when the Run/Step switch is operated,

will be to fetch the instruction from memory

at the address indicated by the P register.

<u>out</u>

<u>IBA</u>

OBA

A, B, C, or D

STARTING THE 8092 TeleProgrammer

- 1) Be sure the TeleProgrammer is plugged into proper power source and room temperature is within the prescribed limits.
- 2) Turn Power switch on power supply to ON.
- 3) Master clear by momentarily pressing Load/Clear switch to Clear.
- 4) When the ERR light goes out, the TeleProgrammer is ready to operate. If repeated master clears do not turn the Red ERR light off, turn off the 8092 and call maintenance.

LOADING A PROGRAM OR DATA

Paper Tape Load Format

- 1) Master Clear
- 2) Turn on reader
- 3) Insert paper tape in reader
- 4) Set P to starting location
- 5) Set Load/Clear switch to LOAD
- 6) Set Run/Step switch to RUN. Paper tape will load and TeleProgrammer will stop.

ENTERING DATA FROM THE TeleProgrammer CONSOLE

- 1) Master clear. Set Enter/Sweep switch to ENTER
- 2) Set P to location into which data is to be entered.
- 3) Enter one word of data into the A register.
- 4) Set Run/Step switch to STEP, once. At this point A is clear and the data word is in storage and in Z.
- 5) If data is to be entered into consecutive locations, go to step 3 and P will be advanced by one on step 4. If data is to be entered into non-consecutive locations, clear P. Go to step 2.

EXAMINING THE STORAGE CONTENTS

- 1) Master clear. Set Enter/Sweep switch on SWEEP
- 2) Set P to location to be examined.
- 3) Press Run/Step switch to STEP, once. The contents of the location specified by P will appear in Z.
- 4) To examine consecutive locations, go to step 3 and P will be advanced by one on step 3. To examine non-consecutive location, clear P, go to step 2.

CHAPTER THREE

A BRIEF LOGICAL DESCRIPTION OF THE TELEPROGRAMMER

Input/Output Section

The input/output (I/O) Section contains one normal (or direct) channel and one buffered channel. Each channel can communicate with five units of peripheral equipment.

The normal channel communicates with external equipment under program control only. There are no provisions for the external equipment to initiate a data transfer except under program control.

The buffered channel communicates with external equipment asynchronously to the main program. It can transfer data in one direction only until changed by program control. In other words, the buffer channel can input to main storage or output from main storage while not under main program control. However, it cannot input and output alternately without having been so instructed by the main program. Once an input buffering or an output buffering operation is initiated, it continues until completed or until cleared by the main program.

The buffer I/O channel has three registers associated with it. These are the Buffer Entrance Register (BER register), the Buffer Exit Register (BXR register), and the Buffer Data Register (BFR register). The BER register holds the buffer starting address and is advanced by one for each buffer cycle. The BXR register holds the buffer ending address, and when BER = BXR the buffer operation is complete. The BFR register holds the input or output

word for transfer to or from external equipment.

The buffer channel may also be used as a normal channel whenever the buffer is not busy.

Interface control is maintained by the control section on a Ready-Resume basis. Within the control section is a separate buffer control section which controls the buffering operations on the same Ready-Resume basis.

Program Step

A program step in the TeleProgrammer is one storage reference cycle. Normally the steps proceed as: 1) Read instruction into control section, 2) Read address of operand (one or two steps) and 3) Perform indicated instruction.

The TeleProgrammer instruction is basically a 2-word instruction contained in 2 sequential storage locations. The first word of the instruction contains: the instruction in the lower 6 bits and the tag bits (TAG register reference bits) in the upper 2 bits. The second word of the instruction contains: the operand (no address mode), the lower 8 bits of a 12-bit address (memory address mode) or the address of one of the first 256 storage locations (indirect address mode).

Arithmetic Section

The arithmetic section of the TeleProgrammer consists of 3 registers and a borrow pyramid. The three registers are the A register, the A' register (which is the accumulator register) and the Z register.

All arithmetic functions (add, subtract and logical operations) are performed by the borrow pyramid which is integrated with the A' register. Inputs to the borrow pyramid are from the A register and the Z register.

Shifting of the A register is accomplished via the borrow pyramid and is confined to a left shift one bit, in the TeleProgrammer. This shifting is a circular shift where the highest order bit is shifted into the lowest order bit position.

The borrow pyramid forms the results of arithmetic operations in a subtractive manner; so that, addition is performed by complementing the Z register and subtracting. Subtraction is a direct process, and logical operations are performed similarly to addition.

Interrupt

The interrupt feature gives the TeleProgrammer four unique interrupt levels which can be utilized in the programming of the TeleProgrammer. The four interrupt levels in order of priority are:

- 1) Manual Interrupt 10
- 2) Buffer Interrupt 20
- 3) External Interrupt 30
- 4) External Interrupt 40

Recognition of an interrupt by the TeleProgrammer forces the TeleProgrammer to start an Interrupt recognition routine which starts at memory location 10 or 20 or 30 or 40 depending on the interrupt activated.

Interruption of the main program can only occur on a 'D' cycle and the occurrence of an interrupt causes the TeleProgrammer to store the address at which it was interrupted and jump to locations 10 or 20 or 30 or 40. At these locations must be the start of a routine which determines the nature of the interrupt. At the end of this routine must be a Clear-Interrupt Lock-out instruction which causes the TeleProgrammer to jump back into the main program at the same address it was at when interrupted. If the interrupt feature is to be used, memory locations 10, 20, 30 or 40 should not be used for the main program or storage.

Interface Control

At the interface of the TeleProgrammer are the same basic control lines and data lines as in the CONTROL DATA 160-A computer.

Storage Section

The storage section of the TeleProgrammer is a high-speed magnetic-core storage system providing non-volatile, random-access storage for 2048 or 4096 8-bit words. Transfer of the words into and out of storage is under control of the control section. For each storage reference cycle, the program-address register (P register) is advanced by 1 to form the address of the next storage location. This address is then entered into the storage access register (S register) where it is translated to a unique selection of one vertical line and one horizontal line selecting 1 core in each of the 8 planes.

After translation, the selected lines are pulsed simultaneously by Read/Write drivers to give a coincident current through the selected core. Normally this would write a "1" in the selected core. If that plane is "inhibited" however, an "0" will be written in that core. The inhibit effectively cancels the effect of the vertical write pulse so that only a half-write current will exist in the core.

Storage Sequence

The storage sequence is divided into four basic portions which accomplish the Read/Write control of the storage section. Every storage sequence is as follows:

- 1) Divert select one of eight vertical and one of eight horizontal lines from the Read/Write drivers.
- 2) Read select one of eight vertical and one of eight horizontal Read/Write drivers in the read mode which drives the core to its "0" state.

- 3) Inhibit cancel the effect of the write pulse and allow the core to remain in the "0" state.
- 4) Write select the same Read/Write driver as on read, and drive the core to its "1" state if the inhibit pulse is absent.

There are two basic registers associated directly with the storage section. These are the storage address register

(S register) and the transfer register (Z register).

The S register is a 12-bit register that holds the storage address during the storage reference cycle. This register has storage capabilities only and is set from the P register, the Buffer Entrance Register (BER register), the A register or the Z register, depending on the instruction being performed.

The Z register is the main transfer and data handling register in the Tele-Programmer. All outputs from the core storage enter the Z or BFR registers, and all inputs to the core storage come from the Z or BFR registers. The Z register also has inputs from the A register, the normal input channel and the buffer input channel in the normal mode. Outputs from the Z register feed the borrow pyramid, the S register, the F register, the normal output channel, and the buffer output channel in the normal mode.

Control Section

The control section of the TeleProgrammer consists of the timing controls, the function translation, and the TAG registers.

Timing Controls

Timing of the operations of the TeleProgrammer is controlled by the timing chain and the primary timing controls. The timing chain is an 8-stage ring counter which recirculates three times for every storage reference cycle to produce a chain of 24, successive, unique pulses. A resynchronizing circuit is employed to insure the timing chain starting on the same clock phase each storage reference cycle.

Function Translation

The instruction control or function control of the TeleProgrammer is achieved by the F register and the function translators. The F register is translated to determine the control and data transfer sequence for any given instruction. The translators are carefully integrated with the timing controls to insure proper operation of the TeleProgrammer.

Address-Tag Registers

Also in the control section are three address-Tag registers each of 4 bits length. These registers are referenced by the tag bits of the instruction word (which are also translated).

The Tag registers are capable of modification at any point in the program from the A register. The upper two bits of the Tag register 3 are used as the buffer channel Tag register. Also, if Tag register 0 is referenced, the address will automatically be one of the first 256 storage locations since Tag register 0 is non-existent.

CHAPTER FOUR

EXTERNAL FUNCTION CODES AND STATUS RESPONSES FOR PERIPHERAL EQUIPMENT

All External Function Codes and Status Responses are given in octal code.

1. 8098 TALLY READER

A. External Function Codes

4102 Select Reader

B. No Status codes

2. 8096 TELETYPE MODEL 33 PAGE PRINTER

A. External Function Codes

4211 Select Input 4221 Select Output

B. No Status codes

3. 350 PAPER TAPE READER

A. External Function Codes

4102 Select Reader

B. No Status codes

4. BRPE-11 PAPER TAPE PUNCH

A. External Function Codes

4104 Select Paper Tape Punch

B. No Status codes

5. <u>161 INPUT/OUTPUT TYPEWRITER</u>

A. External Function Codes

- 4120 Select Typewriter Output
- 4220 Select Typewriter Input
- 4240 Request Typewriter Status

B. Status Response Codes

- 0000 Typewriter Ready
- 0004 Typewriter Power Off
- 0010 Typewriter not in Computer Status
- 0020 Input Character Ready
- 0040 Output in Use

NOTE: If a second typewriter is added, the master octal bits will be 43.

6. 8093 MAGNETIC TAPE SYNCHRONIZER

A. Function Codes

(X) is designated by Unit Select Switch on top of 603 Tape Handler Cabinet. Operator shall use positions 0 through 3.

"Binary" means odd parity is generated and checked on tape. "Coded" means even parity is generated and checked on tape.

- 1X02 Status Request 1
- 1X03 Status Request 2
- 1X07 Programmed Clear
- 1X10 Write, Binary, Low Density
- 1X11 Write, Binary, High Density
- 1X12 Write, Coded, Low Density
- 1X13 Write, Coded, High Density
- 1X14 Write File Mark
- 1X20 Search Forward to File Mark
- 1X21 Search Backward to File Mark
- 1X22 Rewind to Load Point
- 1X24 Search Forward One Record
- 1X25 Search Backward One Record
- 1X26 Rewind Unload
- 1X30 Read, Binary, Low Density
- 1X31 Read, Binary, High Density
- 1X32 Read, Coded, Low Density
- 1X33 Read, Coded, High Density
- 1X34 Read

B. Status Responses

Status Request 1

Bit		
<u>Location</u>	<u>Octal</u>	<u>Description</u>
0	001	Coded (Even Parity, no Odd Parity)
1	002	Transport Not Ready
2.	004	Parity Error
3	010	Illegal Coded on Write (000)
4	020	End of File
5	040	Tape Mark (Load Point or End of Tape)
6	100	High Density (Not Low Density)
7	200	Busy (Tape Motion)
All	277	Program Error

Status Request 2

Octal	Description
001 002	Load Point End of Tape
004	Write Not Ready
010	Searching for File Mark
020	Writing File Mark
	001 002 004 010

7. 162 MAGNETIC TAPE SYNCHRONIZER

A. External Function Codes (6-bit mode, X = 1) (12 bit mode, X = 2)

X110 thru X117	Write if OUT is given. Write End-of-File Mark if no OUT is given.
X120 thru X127	Backspace one record if INA is given. Seach backward to End-of-File Mark if no INA is given.
X120 thru X137	Read forward if INPUT is given. Search forward to End-of-File Mark is no INPUT is given.
X140 thru X147	Request Status

X150 thru Rewind Unload X157 X160 thru Rewind Load X167 X171 Set tapes to odd parity X172 Set tapes to even parity 2100 High density thru 2107 1100 Low density thru 1107

B. Status Response Codes

0000 Odd parity selected - no errors 0001 Even parity selected - no errors 0002 Tape X not ready 0004 Parity error 0015 Illegal BCD detected on Write End-of-File Mark read 0020 0040 End-of-Tape or Load Point sensed 0100 High density 0200 Tape X busy

NOTE: The last octal bit designates one of the four (eight) 60X's. The master octal bits 12, 13, 22, and 23 are used for second and third tape control. If the tape transport is a 606, a 6-bit high density selection is illegal (a programmer consideration).

6. 166-2 LINE PRINTER

A. External Function Codes

0700 Asynchronous print 0710 Synchronous print 0740 Check status 072X Advance forms

B. Status Response Codes

0000 166-2 ready

0001 Buffer busy

0002 Out of paper

0004 Paper moving

0010 Drum stationary

0020 Off-line

9. 167-2 CARD READER (Hollerith Facility)

A. External Function Codes

4500 EF clear

4501 Free run read

4502 Single cycle read

4504 Negate translate, H BCD

4505 FRR, H BCD and pack

4506 SCR, H BCD and pack

4540 Check status

B. Status Response Codes

0000 Card reader ready

0001 Hopper empty

0002 Stacker full

0004 Feed failure

0010 Program error

0020 Amplifier failure

0040 Motor power off

10. 170 CARD PUNCH CONTROL UNIT

A. External Function Codes

3002 Punch

3040 Check Status

B. Status Response Codes

0000 170 ready

0200 MS in 1604 position

2000 Punch not ready

11. 177 CARD READER

A. External Function Codes

```
4500
        EF clear
4501
        Free run read
        Single cycle read
4502
                               BCD, free run read
4505
        Negate translate, H
4506
        Negate translate, H
                             BCD, single cycle read
        Gate card
4510
4540
        Status request
```

B. Status Response Codes

0001 0002	Input tray empty Primary or secondary stacker full
0004	Feed failure
0010	Late input request
0020	Pre-read error
0040	Manual on or motor power off
0100	Read comparison error
0200	End of file
0400	Ready

12. <u>8094 PERIPHERAL ADAPTOR</u>(Required when 12-bit interface is needed for peripheral equipment)

A. External Functions

```
6301 Select
6302 De-Select
```

B. No Status Codes

13. 8060 SERIES DIGITAL COMMUNICATIONS TERMINALS

A. External Function Codes

```
36X0 Select stop send
36X1 Select send
36X2 Select data input
36X3 Select status input
36X4 Select
```

B. Status Response

0000	Computer has	cleared to send
0002	Carrier is on	and computer sending

14. 8095 RECORD TRANSMISSION CONTROL PANEL

A. EXF Codes

35XX Select to input data 3501 Status Request 1 3502 Status Request 2

B. Status Responses #1

The Control Panel will respond with the status responses when the TeleProgrammer sends a 3501 external function.

These status responses are in effect, the way in which the terminal operator communicates with the TeleProgrammer.

Meaning
Send End of Message
Send Come to Phone
End of Message Not Acknowledged
Come to Phone Not Acknowledged
Stop (Not Ready)
Translate
Send Mode (Not Receive)

Response #2

The Control Panel responds with the status responses shown in Table 3 when the TeleProgrammer sends a 3502 external function. This status responses indicates to the TeleProgrammer which peripheral device to select for the input (send) or output (receive) operation it is to perform.

Select Send Switch <u>Position</u>	Octal <u>Response</u>	<u>Select</u>	<u>For</u>
1	0×0	Magnetic Tape	
2	0X1	Punched Cards	
3	0X2	Paper Tape	Sending
4	0X4	I/O Writer	
5	1X1		Equipment
6	1X2		
7	1X4		

Select Send Switch <u>Position</u>	Octal <u>Response</u>	<u>Select</u>	<u>For</u>
1 2 3 4 5 6 7	00X 01X 02X 04X 21X 22X 24X	Receive Device as Called for in Header Magnetic Tape Punched Cards Line Printer Paper Tape I/O Writer	Receiving Equipment

APPENDIX

APPENDIX A

TOSAS -- A TELEPROGRAMMER ASSEMBLER

Preface

The TeleProgrammer is easily programmed in machine language using the previous descriptions and references of this manual. Those Control Data Customers and analysts who have recourse to either a 160 or 160-A Computer, can also use "TOSAS" - the TeleProgrammer One Sixty Assembler System. TOSAS is easily implemented by adopting very slight modifications of the OSAS or OSAS-A assembly language. These modifications are described in this Appendix. Full descriptive manuals of OSAS or OSAS-A are available and can be obtained by writing to:

Industrial Data Processing Division Control Data Corporation 9549 Penn Ave. South Minneapolis, Minnesota

Description of TOSAS

TOSAS uses all the rules of OSAS or OSAS-A. With the exception of minor changes in the coding forms used, along with the adoption of one or two limitations, the two assemblers are the same. The differences are listed in detail below and followed with an example program to indicate the changes.

Providing for Different Function Codes:

The 160 and 160-A Computers employ 6-bit function codes. The TeleProgrammer also uses 6-bit function codes. However, the octal codes are different. To overcome this difference, TOSAS requires a "function Code Identification Listing" as part of the TOSAS program. This identification simply lists the <u>mnemonic codes</u> of the TeleProgrammer under "LOCATION" (cols. 2 - 8 in OSAS coding form); the pseudo OP Code, EQU, under "OP" (cols. 10 - 13); and the TeleProgrammer octal Function Codes under "ADDITIVE" (cols. 23 - 29). "COMMENTS" can appear as usual. A sample of identification listing is shown on page A-6. (The octal addresses in the leftmost column on page A-6 were assigned by the assembler for the problem of which this listing is an example.

Use of "CON"

In OSAS, the pseudo OP, "CON" is used to set aside the first 64 registers (octal address, 0000 through 0077) for constants which follow the code, "CON". In TOSAS, this pseudo OP can be used exactly the same way. However, the TeleProgrammer provides for 256 low core address (octal addresses 0000 through 0377). This means that if the programmer desires to reserve low core area beyond the first 64 locations, he must use separate symbolic tags under "LOCATION" preceded by the pseudo OP, "PRG" or by using the EQU pseudo OP as shown.

Example: Assume one wants to store octal constants: 5, 27, 31 and LG at respective octal locations 0076, 0077, 0100 and 0101.

LOCATION	<u> </u>	ADDRESS	<u>ADDITIVE</u>	COMMENTS
	CON	76		
			5	
			27	
	PRG	100		
			31	
LG	EQU	101		

Size of Numerics Under ADDITIVE Column

Since the TeleProgrammer involves an 8-bit word length instead of 12 bits, the size of the octal numbers (quantities and addresses) must not exceed 8 bits. Thus, the effective range is 000 through 377. In addition, 100, 200, or 300, must appear in the ADDITIVE column opposite the mnemonic code to indicate respectively the use of Tag registers 1, 2, or 3. (See examples.)

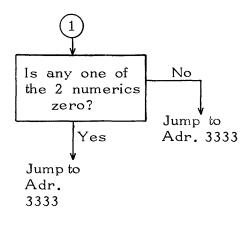
Difference in Coding

The same coding forms, as used in OSAS or OSAS-A, can be used in TOSAS. The difference is in the placement of mnemonic OP codes. In TOSAS, all TeleProgrammer mnemonic OP codes are placed under the "ADDRESS" column rather than the "OP" column. Symbolic addresses can be placed under the mnemonic, in the "ADDRESS" column, or in the "ADDITIVE" column. Octal numerics or decimal numerics (with letter "D") can be placed under "ADDITIVE". Also, 100, 200, or 300 must appear in the ADDITIVE column directly opposite the mnemonic code of the ADDRESS column to respectively indicate use of Tag register 1, 2, or 3. Thus in the example on the next page the third line of coding LDM 200 106 indicates that Tag register 2 is used with LDM, and contains the upper 4 bits of address 106 which follows.

To aid the reader in the TOSAS concept, a sample example is programmed, using TOSAS. A few sheets of the routine, on OSAS coding form, and the corresponding TOSAS listing are shown on pages A-7 through A-12. (Since this example used the lower 256 core memory locations, the reader should note that the use of 100, 200, or 300 opposite the mnemonic codes is reserved for the occasions when jumps or references beyond the first 256 registers are made. In such instances, Tag registers are required.

Example: Assume octal address 3106 and 3107 contain unknown numerics. If any one of these numerics is zero, jump to address, 3255; otherwise, jump to T1 (where T1 = Adr. 3333).





TeleProgrammer Octal Code

{0LDN 0 0 6 2ATT }	Store octal, 3, in three left bits of Tag Reg. 2
$ \left\{ \begin{array}{c} 2LDM \\ 1 06 \end{array} \right\} $	Contents of Adr. 3106 to A
$ \left\{ \begin{array}{c} 2ZJP \\ 255 \end{array} \right\} $	If zero, jump to Adr. 3255
$ \left\{ \begin{array}{c} 2 L D M \\ 1 0 7 \end{array} \right\} $	Contents of Adr. 3107 to A
$ \left\{ \begin{array}{c} 2ZJP \\ 255 \end{array} \right\} $	If zero, jump to Adr. 3255
2UJP }	Jump to Adr. 3333

TOSAS Coding (using OSAP Coding Form)

LOCATION	OP	ADDRESS	ADDITIVE	COMMENTS
		LDN		Octal 3 to Tag Reg. 2
			6	
		ATT	200	
		LDM	200	Contents of Adr. 3106 to A
			106	
		ZJP	200	If zero, jump to 3255
			255	
		LDM	200	Contents of Adr. 3107 to A
			107	
		ZJP	200	If zero, to Adr. 3255
			255	
		UJP		Jump to T1
		T1*		

^{*} Where T1 must be previously identified in the program by a statement such as: <u>LOCATION</u> <u>OP ADDRESS</u>

T1 EQU 3333

IDENTIFICATION LISTINGS

	Location	<u>op</u>	Additive	Comments
0000	ERR	EQU	0	ERROR STOP
0001	SHA	EQU	ŧ	SHIFT A LEFT ONE BIT
0002		EQU	2	A TO TAG REGISTER
0003		EQU	3	TAG REGISTER CONTENTS TO A
0004	ABR	EQU	4	A TO BUFFER ENTRANCE REGISTER
0005		EQU	5	A TO BUFFER EXIST REGISTER
0006	BER	EQU	6	CONTENTS OF BER REGISTER TO A
0007	CBC	EQU	7	CLEAR BUFFER CONTROLS
0010		EQU	10	LOGICAL PRODUCT NO ADDRESS
0011	LPM	EQU	11	LOGICAL PRODUCT MEMORY ADDRESS
0012	LPI	EQU	12	LOGICAL PRODUCT INDIRECT ADDRESS
0013	CIL	EQU	13	CLEAR INTERRUPT LOCKOUT
0014	LSN	EQU	14	LOGICAL SUM NO ADDRESS
0015		EQU	15	LOGICAL SUM MEMORY ADDRESS
0016	LSI	EQU	16	LOGICAL SUM INDIRECT ADDRESS
0020	LON	EQU	20	LOAD A NO ADDRESS MODE
0021	LUM	EQU	21	LOAD A MEMORY
0022	LOI	EQU	22	LOAD A INDIRECT
0025	LCM	EQU	25	LOAD COMPLEMENT TO A MEMORY
0026	LCI	EQU	26	LOAD COMPLEMENT TO A INDIRECT
0030	ADN	EQU	30	ADD NO ADDRESS
0031	MÜA	EQU	31	AUD MEMORY ADDRESS
0032	ADI	EQU	32	ADD INDIRECT ADDRESS
0034	SBN	EQU	34	SUBTRACT NO ADDRESS
0035	SBM	EQU	35	SUBTRACT MEMORY ADDRESS
0036	SBI	EQU	36	SUBTRACT INDIRECT ADDRESS
0041	STM	EQU	41	STORE A MEMORY
0042	STI	EQU	42	STORE A INDIRECT
0051	RAM	EQU	51	REPLACE ADD MEMORY ADDRESS
0055	RAO	EQU	55	REPLACE ADD ONE MEMORY ADDRESS
0060	ZJB	EQU	60	JUMP : IF CONTENTS OF A = 0
0061	NZP	EQU	61	JUMP: IF CONTENTS OF A (O
0062	PJP	EQU	62	JUMP: IF CONTENTS OF A O POSITIVE
0063	NJP	EQU	63	JUMP: IF CONTENTS OF A O NEGATIVE
0064	UJP	EQU	64	UNCONDITIONAL JUMP
0070		EQU	7 0	INITIATE BUFFER INPUT
0071	180	EQU	71	INITIATE BUFFER OUTPUT
0072		EQU	72	INPUT NORMAL
0073		EQU	73	OUTPUT NORMAL
0074		EQU	74	OUTPUT: NO ADDRESS
0075		EQU	75	EXTERNAL FUNCTION
0076		EQU	76	INPUT TO A
0077		EQU		HALT
0000		END	. ,	COMPLETE ASSEMBLY



OSAS/OSAS-A CODING FORM

A TOSAS Assembly Program (Part of "XLATE" Routine)

PAGE NO. ______
DATE _____
PROGRAMMER _____

₂ LOCATION	10 OP	15 ADDRESS	23 ADDITIVE	COMMENTS
I, N, P, U, T, A,		LDM,	1	ROUTINE M/T INPUT A
			F, L, A, G, 1, ,	
		$Z_1J_1B_1$		TEST FLAG IF 1st TIME
	1 1		I , N, P, U, T, 1,	NO JUMP
		L,D,N,\dots		
			0,	
		STM		
			F, L, A, G, 1, ,	T/H STATUS
		E, X, F,	1 1	
			$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	RS1
		INA	0,41 1 1 1	
		S _. B _. N _.		TEST IF T/H ON
			$4 \cdot 1 \cdot \cdot \cdot \cdot$	LØAD PØINT AND CØDE
		N ₁ Z ₁ P ₁		BELLE I PHAT THAT OF EL
			I , N, P, U, T, 2,	NOT READY
I, N, P, U, T, 1		E,X,C,	V-7	T/H STATUS
			1,1,,,,,	RS1
	1_11	1 1 1 1 1	0,2, , , , ,	
	11	I, N , A , , , ,		
		L _i P _i N _i		SAVE BUSY BIT
			2,0,2, , , ,	
		$N_iZ_iP_i$		TDV ACADI
			I , N, P, U, T, 1	TRY AGAIN
I, N, P, U, T, 6,	1 1	E, X, F, \dots	1,1,,,,,	READ BCD LOW
			$\frac{1}{3}, \frac{1}{2}, \dots, \frac{1}{3}$	READ BCD LOW
		I ,N,N, , ,	3,0,0, , ,	
			F, W, A,	
	141		L, W, A,	
I , N, P, U, T, 3		E,X,F,		TAKE STATUS ØF
			1,1	READ
FORM 138 - REPLACES 138 a	ь Use shade	d columns only if f	irst symbol characte	er is + or -, or for 4 character OP code

P-3



OSAS/OSAS-A CODING FORM PAGE NO. _____ DATE _____ PROGRAMMER __ 10 OP **ADDRESS ADDITIVE** COMMENTS LOCATION 31 $0.2_{-1.1}$ $I_1N_1A_1$ STORE STATUS $S_{l} T_{l} M_{l}$ $T_1E_1M_12$ LPN 2,0,0, N, Z, PN,P,U,T, 2 LOAD STATUS LD, M $T_1 E_1 M_1 2_1$ BACK IN L, P, N 2,4,, SAVE EØF & PARITY $Z_i J_i B_i$ 1,0,0, W,O,R,K,JUMP TO WORK ROUTINE L, P, N SAVE PARITY BIT 0,4, $N_i Z_i P_i$ I, N, P, U, T, 4, JUMP TO EØM ROUTINE 3,0,0, u.J.P. $E, \emptyset, M,$ I N.P.U.T.2 SET RETURN LP N 6.3. . . JUMP FOR S. T. M. 3,0,0, LOCAL TROUBLE R, E, T, U, R, NL.D.N. I, N.P. U.T. 1. 3_0_0, ___ $S_1T_1M_1$ $J_1U_1M_1P_1$ JUMP TO LOCAL TROUBLE u,j,P, 3,0,0, L,O, T, R,O, U, ROUTINE PARITY ON READ , N. P. U. T. 4. $E_{i}X_{i}F_{i}$ 1.1.

8



OSAS/OSAS-A CODING FORM PAGE NO. DATE _____ PROGRAMMER. 10 OP **ADDRESS** LOCATION ADDITIVE COMMENTS 2,5, , BACK SPACE ONE RECORD $L_{i}D_{i}M_{i}$ T, R, Y, 3, $N_i J_i P_i$ I, NP, U, T, 5, $S_1H_1A_1$ S, T, M, STØRE BACK AT $T_1R_1Y_13_1$ TRY 3 $U_1J_1P_1$ INPUT, 6, READ AGAIN $L_{i}D_{i}N_{i}$ SET TRY 3 0,2,1, $S_{L}T_{L}M_{L}$ T, R, Y, 3, $L_1D_1N_1$ 0, 6, 3, 3, 0, 0, , , $S_{1}T_{1}M_{1}$ R,E,T,U,R,1, $L_1D_1N_1$ I NPUT6 3, 0, 0, , , S. T. M. $J_1U_1M_1P_11_1$ U,JP, 3, 0, 0, , T,I,M,E, $P_{i}R_{i}G$ 4,0,0,

FORM 1380 - REPLACES 1380 &b Use shaded columns only if first symbol character is + or -, or for 4 character OP code

Listing From Previous TeleProgrammer "XLATE" Routine

0130	0021	INPUTA	LDM		ROUTINE M/T INPUTA
0131	0060		P	FLAGI	
0132	0060		ZJB		TEST FLAG IF IST TIME
0133	0173			INPUTI	NO JUMP
0134	0020		LON		
0135	0000			0	
0136	0041		STM		
0137	0060			FLAGI	
0140	0075	INPUT7	EXF		TAKE STATUS OF TAPE
0141	0011			11	
0142	0002			2	
0143	0076		INA		
0144	0041		STM		SAVE STATUS
0145	0066			TEM4	
0146	0010		LPN		SAVE NOT READY BIT
0147	0002			2	
0150	0061		NZP		TAPE NOT READY
0151	0237			INPUT2	
0152	0021		LDM		BRING STATUS BACK
0153	0066			TEM4	
0154	0010		LPN		IS IT BUSY
0155	0200			200	
0156	0061		NZP		YES TRY AGAIN
0157	0140			INPUT7	
0160	0021		LDM		
0161	0066		TEM4		BRING STATUS BACK
0162	0034		SBN		CHECK LOAD POINT
0163	0041			41	
0164	0060		ZJB		GO ON TO READY
0165	0203			INPUTE	
0166	0075		EXF		REWIND TAPE TO LOAD POINT
0167	0011			TI	
0170	0022			22	
0171	0064		UJP		GO TAKE STATUS AGAIN
0172	0140			INPUT7	
0173	0075	INPUTI	EXF		T/H STATUS
0174	0011			11	RSI
0175	0002			2	
0176	0076		INA		
0177	0010		LPN		SAVE BUSY BIT
0200	0202			202	
0201	0061		NZP		
0202	0173			INPUTI	TRY AGAIN

TeleProgrammer "XLATE" Routine Listing (Con't)

0203	0075	INPUTE	EXF		· · · · · · · · · · · · · · · · · · ·
0204	0011			11	
0205	0032			32	READ BCD LOW
0206	0372		INN	300	
0207	0000			0	FWA
0210	0120			120	LWA
0211	0075	INPUT3	EXF		TAKE STATUS OF
0212	0011			11	READ
0213	0002			2	
0214	0076		INA		
0215	0041		STM		STORE STATUS
0216	0064			TEM2	
0217	0010		LPN		
0220	0200			200	
0221	0061		NZP		
0222	0211			INPUT3	LAAD OTATUO
0223	0021		LDM		LOAD STATUS
0224	0064			TEM2	BACK IN
0225	0010		LPN	5 //	CAUE FOR AND DADLEY
0226	0024		7.10	24	SAVE EOF AND PARITY
0227	0160		ZJB	100	HIMP TO HOOK DOUTING
0230	1213			WORK	JUMP TO WORK ROUTINE
0231	0010		LPN	44	CAUE DIDITY OIT
0232	0004	,	NZD	4	SAVE PARITY BIT
0233	0061		NZP	INPUT4	
0234	0251		UJP		JUMP TO EOM ROUTINE
0235	0364		UJP	300 EOM	JUMP TO EUM ROUTINE
0236	0676	INPUT2	LDN	EUN	SET RETURN
0237	0020 0063	INPUIZ	LUN	63	JUMP FOR
0240	0341		STM	300	LOCAL TROUBLE
			3111	RETURN	FOCKE INDOBEE
0242	0652		LDN	RETURN	
0243	0173		LDN	INPUTI	
0245	0341		STM	300	
0245	0653		3111	JUMP	
0247	0364	· · · · · · · · · · · · · · · · · · ·	UJP	300	JUMP TO LOCAL TROUBLE
0247	0636		001		ROUTINE
0251	0075	INPUT4	EXF		PARITY ON READ
0251	0011	1111 014	471	11	Trickett with News
0252	0025			25	BACK SPACE ONE RECORD
0254	0021		LDM		
0255	0115			TRY3	
0256	0063		NJP		
0257	0265			INPUT5	
0260	0001		SHA		
0261	0041		STM		STORE BACK AT
0262	0115			TRY3	TRY3
					

TeleProgrammer "XLATE" Routine Listing (Con't)

0263	0064		UJP	
0264	0173			INPUTI READ AGAIN
0265	0020	INPUT5	LON	
0266	0021			21
0267	0041		STM	SET TRY 3
0270	0115			TRY3
0271	0020		LDN	
0272	0063			63
0273	0341		STM	300
0274	0672			RETURI
0275	0020		LDN	
0276	0173			INPUTI
0277	0341		STM	300
0300	0673			JUMPI
0301	0364		UJP	300
0302	0656			TIME

The previous listing is <u>part</u> of a Magnetic Tape input routine. As such, the reader should be aware of the fact that several symbolic tags are used (for example, FLAG 1, TEM 2, TEM 4, WORK, etc.) which were identified by "EQU" statements on other parts of the total program. Likewise, notes, page number, etc. refer to the total program from which the example was taken.

APPENDIX B

PROGRAMMING EXAMPLES

Example 1 Servicing the Interface

A small message switching system is composed of ten full duplex lines operating at rates of 100 words per minute. Each time the input interface is serviced (once each 100 milliseconds) each of the ten input terminal units (TTU) supplies one 8 bit character, where each character contains 7 bits of data and 1 parity bit).

The octal select codes of the ten TTU units are identical to the octal memory addresses that are used to store the inputs. These addresses are:

0420	0425
0421	0426
0422	0427
0423	0430
0424	0431

Each time the input interface is serviced, <u>one</u> character from each of the ten TTU locations is read into a corresponding Raw Data Register (RDR) in the TeleProgrammer memory. Assuming the Raw Data registers start at octal address, 0600, the program follows:

Program Location		uctions Codes	Cycles	Action Performed
0460 0461	0	LDN 01	} 2	Load A with 1
0462	1	ATT	} 1	Bits, 001, go to Tag reg. 1
0463 0464 0465	0 0 0	EXF 04 20	} 3	Select the TTU, starting with the first TTU.
0466	0	INA	} 2	Input the character from the selected TTU to the A register.
0467 0470	$\begin{bmatrix} 1 \\ 2 \end{bmatrix}$	STM 00	} 3	Store character in A at desired memory location
0471 0472	1 0	RAO 70	} 4	Add 1 to memory location where characters are stored.
0473 0474	1 0	RAO 65	} 4	Add 1 to TTU select address. This also tests last TTU address.
0475 0476	0	SBN 32	} 2	Subtract one more than number of lines being serviced.
0477 0500	1 0	NJP 63	} 2	If not last servicing, jump back to service next TTU.
0501	Coi	ntinue		

^{*} Note: The above instructions contain mnemonic function codes in order to indicate the type of instruction being performed. Before program execution, these must be replaced by their equivalent numeric codes.

Example 2 Assuring Transmission Validity

Several techniques have evolved to assure message content validity.

One such technique is a form of the Fire code which is described in the following problem. By this method, specific words of the data to be transmitted are added into eight "Check Sum" (S) words. After computing each of the eight sum words, at both origin and destination locations, comparisons of the corresponding sums indicate message validity. This technique provides the advantage of being able to use all bits of a message character as information bits. Thus the presence of a parity bit is not mandatory. However, the presence of a parity bit does not affect or degrade the method.

Assume a block of 240 words of 1 character per word is to be transmitted. This block is preceded by an 8 word header, and followed by 8 Check Sum words. Using a Fire code, the data in the header and information portions are to be checked through comparisons of the accumulated sums in the 8 Check Sum (S) words. The accumulated sums of the sum words are determined by the following algorithm:

$$S_{1} = W_{i} + W_{j} + W_{k} + ---- + W_{n}$$

$$S_{2} = W_{i+1} + W_{j+1} + W_{k+1} + --- + W_{n+1}$$

$$S_{3} = W_{i+2} + W_{j+2} + W_{k+2} + --- + W_{n+2}$$

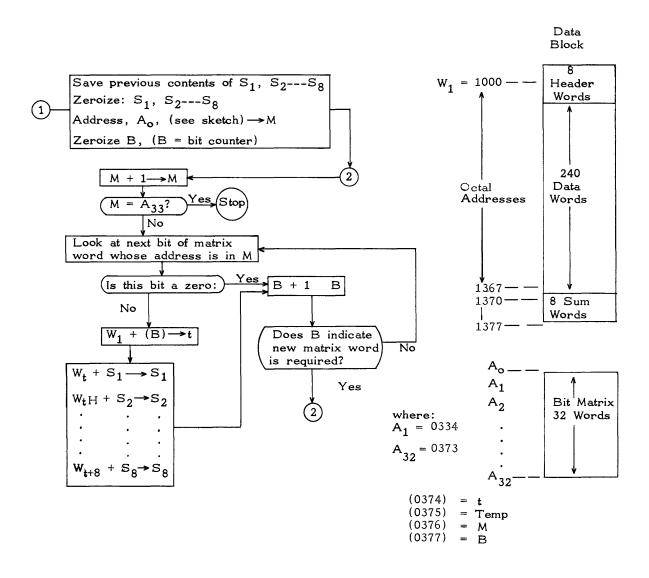
$$S_{8} = W_{i+7} + W_{j+7} + W_{k+7} ---- + W_{n+7}$$

where i,j,k, --- n are the computer addresses containing the data words which are to be transmitted.

W = data words, thus $W_j = data word at address j$ S_1 , S_2 , --- $S_8 = Check Sum words$

In order to implement this method, a matrix of 32 words is used. Each of the 32 words contains 8 bits which indicate the computer addresses of the words which are to be added in the <u>first</u> Check Sum word, S_1 . Thus the bit locations within the matrix indicates: i, j, k, ---n addresses of the preceding algorithm.

The technique is indicated by the flow chart and diagram of TeleProgrammer areas below:



THE PROGRAM

Location	<u>T</u>	Code	C	vcles	Action Performed
2000 2001	1 -	LDN 02	}	1	Preset Tag register 1 to 0010 (in bits)
2002	1	ATT	}	1	-
2003 2004 2005 2006 2007 2010 2011 2012 2013 2014 2015 2016	3 0 3 2 0 2 0 0 3 2	LDM 70 STM 24 RAO 04 RAO 06 SBN 34 NZP 03	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	3 4 4 2 2	Save the contents of the check sum words by storing initial contents at following addresses: $S_1 \longrightarrow 0324$ $S_2 \longrightarrow 0325$ $S_8 \longrightarrow 0333$
2017 2020 2021 2022	1	LDN 00 STM 70	}	2	This loop presets each of the eight check sum words to zero.
2023 2024 2025 2026	0 2	 RAO 22 NZP 17 	}	4 2	
2027 2030		STM 77 	}	3	Set Bit Counter, B, to zero. (B is located at octal address, 377.)

THE PROGRAM

Location	T Code	Cycles	Action Performed
2031 2032 2033 2034	0 LDN 3 33 0 STM 3 76	} 2 3	Store first address minus 1 of Bit Matrix at M; where M is at address 0376.
2035 2036	0 RAO 3 76	} 4	M + 1 → M
2037 2040 2041 2042	0 SBN 3 74 2 ZJP 1 12	} 2	Test address at M, and jump if last Matrix Word has been serviced.
2043 2044	0 LDI 3 76	} 4	Load next Matrix Word into A
2045	0 SHA	} 1	Shift Matrix Word left 1
2046 2047	0 STM 3 75	} 3	Store shifted Matrix Word at tempo- rary register (at address 0375).
2050 2051	0 LPN 0 001	} 2	Look at what previously had been the leftmost bit of Matrix Word.
2052 2053	2 NZP 0 66	} 2	If bit ≠ 0, jump; otherwise, continue.
2054 2055	0 RAO 3 77	} 4	B + 1→B (Increase bit count by 1.)
2056 2057	0 LPN 0 07	} 2	Look at last three bit positions of count at B.

THE PROGRAM

			1	
Location	工	Code	Cycles	Action Performed
2060 2061	2	ZJP 35	} 2	If next Matrix Word is required, jump. Otherwise, continue.
2062 2063 2064 2065	0 3 2 0	LDM 75 UJP 45	} 3 2	Return the current Matrix Word to A and jump back to look at next bit.
2066 2067 2070 2071	0 3 0 3	LDM 77 STM 74	} 3	Bit Count → t, where t is at address 0374.
2072 2073 2074 2075	1 3 1 3	LDI 74 RAD 70	} 4	$W_t + S_1 \longrightarrow S_1$
2076 2077 2100 2101	0 3 2 0	RAO 74 RAO 75	} 4	Update parameters in above equation.
2102 2103	2	 _{NZP} 72	} 2	Loop back to location, 2072, if not zero.
2104 2105 2106 2107		LDI 74 RAD 77	} 4	Store into last Check Sum Word at address 0777.
2110 2111	2 0	UJP 54	} 2	Loop back for next iteration.
2112	0	HLT	} 1	Stop

APPENDIX C - MATHEMATICAL TABLES

TABLE OF POWERS OF TWO

```
2" n 2-"
             1
                 0 10
             2
                 1 0.5
                 2 0.25
             8
                 3 0.125
            16
                 4 0.062 5
            32
                 5 0.031 25
            64
                 6 0.015 625
           128
                 7 0.007 812 5
                 8 0.003 906 25
           256
           512
                    0.001 953 125
                10 0.000 976 562 5
         1 024
         2 048
                11 0.000 488 281 25
         4 096
                12 0.000 244 140 625
                13 0.000 122 070 312 5
         8 192
         16 384
                14 0.000 061 035 156 25
        32 768
                15 0.000 030 517 578 125
        65 536
                16 0.000 015 258 789 062 5
       131 072
                17 0.000 007 629 394 531 25
       262 144
                18 0.000 003 814 697 265 625
       524 288
                19 0.000 001 907 348 632 812 5
     1 048 576
                20 0.000 000 953 674 316 406 25
     2 097 152
                21
                    0.000 000 476 837 158 203 125
     4 194 304
                22 0.000 000 238 418 579 101 562 5
     8 388 608
                    0.000 000 119 209 289 550 781 25
    16 777 216
               24 0.000 000 059 604 644 775 390 625
    33 554 432 25 0.000 000 029 802 322 387 695 312 5
    67 108 864 26 0.000 000 014 901 161 193 847 656 25
   134 217 728
                27
                   0.000 000 007 450 580 596 923 828 125
   268 435 456 28
                    0.000 000 003 725 290 298 461 914 062 5
   536 870 912 29
                    0.000 000 001 862 645 149 230 957 031 25
 1 073 741 824
                30
                    0.000 000 000 931 322 574 615 478 515 625
 2 147 483 648
                    0.000 000 000 465 661 287 307 739 257 812 5
 4 294 967 296
                    0.000 000 000 232 830 643 653 869 628 906 25
                32
 8 589 934 592
                33
                    0.000 000 000 116 415 321 826 934 814 453 125
                    0.000 000 000 058 207 660 913 467 407 226 562 5
17 179 869 184
                34
34 359 738 368
                    0.000 000 000 029 103 830 456 733 703 613 281 25
                35
68 719 476 736 36
                    0.000 000 000 014 551 915 228 366 851 806 640 625
                    0.000 000 000 007 275 957 614 183 425 903 320 312 5
137 438 953 472
274 877 906 944 38 0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888 39 0.000 000 000 001 818 989 403 545 856 475 830 078 125
```

		0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
0000 0000	0000	0000	0001	0002	0003	0004	0005	0006	0007	(0400	0256	0257	0258	0259	0260	0261	0262	0263
to to	0010	8000	0009	0010	0011	0012	0013	0014	0015		0410	0264	0265	0266	0267	0268	0269	0270	0271
0777 0511	0020	0016	0017	0018	0019	0020	0021	0022	0023		0420	0272	0273	0274	0275	0276	0277	0278	0279
(Octal) (Decimal)	0030	0024	0025 0033	0026 0034	0027	0028 0036	0029 0037	0030	0031		0430	0280 0288	0281 0289	0282 0290	0283 0291	0284 0292	0285 0293	0286 0294	0287 0295
	0050	0032	0033	0034	0035 0043	0036	0045	0046	0039		0440	0296	0209	0290	0299	0300	0293	0302	0303
	0060	0048	0049	0050	0051	0052	0053	0054	0055		0460	0304	0305	0306	0307	0308	0309	0310	031
Octal Decimal	0070	0056	0057	0058	0059	0060	0061	0062	0063		0470	0312	0313	0314	0315	0316	0317	0318	0319
10000 - 4096									ļ										
20000 - 8192	0100	0064	0065	0066	0067	0068	0069	0070	0071		0500	0320	0321	0322	0323	0324	0325	0326	0327
30000 - 12288	0110	0072	0073	0074	0075	0076	0077	0078	0079		0510	0328	0329	0330	0331	0332	0333	0334	0335
40000 - 16384	0120	0800	0081	0082	0083	0084	0085	0086	0087		0520	0336	0337	0338	0339	0340	0341	0342 0350	0343
50000 - 20480	0130	0088 0096	0089 0097	0090 0098	0091 0099	0092 0100	0093	0094 0102	0095		0530 0540	0344 0352	0345 0353	0346 0354	0347 0355	0348 0356	0349 0357	0358	035 035
60000 - 24576	0150	0104	0105	0106	0107	0108	0109	0110	0111	1	0550	0360	0361	0362	0363	0364	0365	0366	036
70000 - 28672	0160	0112	0113	0114	0115	0116	0117	0118	0119		0560	0368	0369	0370	0371	0372	0373	0374	037
	0170	0120	0121	0122	0123	0124	0125	0126	0127		0570	0376	0377	0378	0379	0380	0381	0382	0383
									1										
	0200	0128	0129	0130	0131	0132	0133	0134	0135		0600	0384	0385	0386	0387	0388	0389	0390	039
	0210	0136	0137	0138	0139	0140	0141	0142	0143		0610	0392	0393	0394	0395	0396	0397	0398	039
	0220	0144	0145	0146	0147	0148	0149	0150	0151		0620	0400	0401	0402	0403	0404	0405	0406	040
	0230	0152	0153	0154	0155	0156	0157	0158 0166	0159		0630	0408 0416	0409 0417	0410 0418	0411 0419	0412	0413 0421	0414 0422	0419
	0240 0250	0160 0168	0161 0169	0162 0170	0163 0171	0164 0172	0165 0173	0166	0167 0175		0640 0650	0416	0417	0418	0419	0420 0428	0421	0422	042
	0260	0176	0103	0178	0179	0172	0173	0182	0173		0660	0432	0423	0434	0435	0436	0423	0438	043
	0270	0184	0185	0186	0187	0188	0189	0190	0191		0670	0440	0441	0442	0443	0444	0445	0446	044
	0300	0192	0193	0194	0195	0196	0197	0198	0199		0700	0448	0449	0450	0451	0452	0453	0454	045
	0310	0200	0201	0202	0203	0204	0205	0206	0207		0710	0456	0457	0458	0459	0460	0461	0462	046
	0320	0208	0209	0210	0211	0212	0213	0214	0215		0720	0464	0465	0466	0467	0468	0469	0470	047
	0330	0216	0217	0218	0219	0220	0221	0222	0223		0730	0472 0480	0473	0474	0475 0483	0476 0484	0477 0485	0478 0486	047
	0340 0350	0224 0232	0225 0233	0226 0234	0227 0235	0228 0236	0229 0237	0230 0238	0231		0740 0750	0480	0481 0489	0482 0490	0483	0484	0493	0494	049
	0360	0232	0233	0234	0233	0230	0237	0246	0233		0750	0496	0403	0498	0499	0432	0501	0502	0503
	0370	0248	0249	0250	0251	0252	0253	0254	0255		0770	0504	0505	0506	0507	0508	0509	0510	051
		1									1						, , , , , , , , , , , , , , , , , , ,	-	
		0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
1000 0512	1000	0	1 0513																
1000 0512	1000	O 0512	0513	0514	0515	0516	0517	0518	0519		1400	0768	0769	0770	0771	0772	0773	0774	0775
to to	1010 1020	0 0512 0520 0528	0513 0521 0529	0514 0522 0530	0515 0523 0531	0516 0524 0532	0517 0525 0533	0518 0526 0534	0519 0527 0535		1400 1410 1420	0768 0776 0784	0769 0777 0785	0770 0778 0786	0771 0779 0787	0772 0780 0788	0773 0781 0789	0774 0782 0790	0775 0783 0791
to to 1777 1023	1010 1020 1030	0 0512 0520 0528 0536	0513 0521 0529 0537	0514 0522 0530 0538	0515 0523 0531 0539	0516 0524 0532 0540	0517 0525 0533 0541	0518 0526 0534 0542	0519 0527 0535 0543	:	1400 1410 1420 1430	0768 0776 0784 0792	0769 0777 0785 0793	0770 0778 0786 0794	0771 0779 0787 0795	0772 0780 0788 0796	0773 0781 0789 0797	0774 0782 0790 0798	0775 0783 0791 0799
to to	1010 1020 1030 1040	0 0512 0520 0528 0536 0544	0513 0521 0529 0537 0545	0514 0522 0530 0538 0546	0515 0523 0531 0539 0547	0516 0524 0532 0540 0548	0517 0525 0533 0541 0549	0518 0526 0534 0542 0550	0519 0527 0535 0543 0551		1400 1410 1420 1430 1440	0768 0776 0784 0792 0800	0769 0777 0785 0793 0801	0770 0778 0786 0794 0802	0771 0779 0787 0795 0803	0772 0780 0788 0796 0804	0773 0781 0789 0797 0805	0774 0782 0790 0798 0806	0775 0783 0791 0799
to to 1777 1023	1010 1020 1030 1040 1050	0 0512 0520 0528 0536 0544 0552	0513 0521 0529 0537 0545 0553	0514 0522 0530 0538 0546 0554	0515 0523 0531 0539 0547 0555	0516 0524 0532 0540 0548 0656	0517 0525 0533 0541 0549 0557	0518 0526 0534 0542 0550 0558	0519 0527 0535 0543 0551 0559		1400 1410 1420 1430 1440 1450	0768 0776 0784 0792 0800 0808	0769 0777 0785 0793 0801 0809	0770 0778 0786 0794 0802 0810	0771 0779 0787 0795 0803 0811	0772 0780 0788 0796 0804 0812	0773 0781 0789 0797 0805 0813	0774 0782 0790 0798 0806 0814	0775 0783 0791 0799 0807
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7010 7020 7050 7060 7070 7100 71100 7120 7130 7140 7220 7220 7220 7220 7220 7270 7300 7310 7310 7310 7310 7310 7310 73	3584 3592 3600 3608 3616 3624 3632 3640 3672 3680 3704 3712 3720 3728 3736 3744 3752 3768 3768 3776 3768	3586 3593 3601 3609 3617 3625 3633 3641 3649 3665 3673 3705 3713 3721 3721 3745 3769 3777 3785 3769 3777 3785 3777 3785 3783 3783 3783 3783	3586 3594 3602 3610 3618 3624 3650 3658 3674 3698 3706 3714 3722 3730 3738 3746 3754 3776 3776 3778 3786 3778	3587 3595 3603 3611 3627 3635 3663 3663 3675 3675 3707 3715 3723 3731 3747 3753 3771 3779 3787 3785	3588 3588 3604 3612 3628 3636 3644 3652 3700 3708 3716 3732 3740 3748 3772 3780 3782 3780 3788 3788 3788	3589 3497 3605 3613 3629 3637 3645 3653 3669 3677 3683 3701 3709 3717 3725 3733 3741 3749 3773 3781 3783 3781 3783 3781 3783	3590 3698 3606 3614 3622 3630 3638 3646 3652 3670 3718 3726 3734 3742 3750 3774 3782 3790 3788 3798 3798	3591 3599 3607 3615 3623 3631 3639 3655 3663 3671 3679 3772 3735 3743 3751 3759 3793 3791 3793 3793 3793 3793 3793 379	7410 7420 7430 7440 7450 7460 7460 7500 7510 7520 7530 7540 7550 7660 7670 7700 7710 7720 7730	3840 3848 3856 3864 3872 3880 3912 3920 3936 3936 3943 3952 3952 3960 4000 4000 4004 4044 4044 4044 4044 4	3841 3849 3857 3865 3873 3881 3993 3993 3993 3993 3993 3993 4001 4002 4003 4041 4044 4049 4047	3842 3850 3858 3866 3874 3892 3994 3932 3938 3944 3962 3970 3978 4002 4014 4002 4014 4026	3843 3851 3859 3867 3875 3883 3891 3923 3931 3939 3947 3963 3971 3987 4003 4011 4027 4043 4054	3844 3852 3860 3868 3876 3884 3990 3916 3932 3940 3940 3954 3954 4004 4012 4024 4052 4036 4044 4050	3845 3853 3861 3869 3877 3885 3893 3901 3908 3917 3925 3933 3941 3949 4005 4013 4005 4013 4029 4037 4045 4053 4061	3846 3854 3862 3870 3886 3894 3902 3910 3926 3934 3945 3953 3958 3958 3966 3974 4039 4004 4022 4030 4038 4046 4054 4062	3847 3855 3863 3871 3887 3893 3903 3911 3919 3935 3943 3959 3967 3983 3991 4007 4015 4023 4031 4047 4053	to 7777	to 4095
7010 7020 7050 7060 7070 7100 7110 7120 7130 7140 7150 7170 7200 7210 7210 7220 7230 7240 7250 7270 7300 7310 7320 7330 73340	3584 3592 3600 3616 3624 3652 3640 3652 3664 3652 3672 3688 3696 3704 3712 3720 3736 3744 3752 3760 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3764	3585 3593 3601 36019 3617 3625 3633 3641 3687 3681 3689 3793 3705 3713 3729 3745 3753 3761 3769 3777 3785 3793 3809	3586 3594 3602 3610 3626 3634 3650 3658 3666 3774 3778 3778 3778 3778 3778 3778 3778	3587 3595 3603 3611 3627 3635 3663 3661 3659 3663 3691 3707 3715 3763 3763 3763 3763 3771 3779 3787 3787 3787 3787 3787 3787 3883	3588 3496 3604 3612 3628 3636 3644 3692 3700 3712 3748 3748 3756 3764 3772 3780 3788 3798 3798	3589 3497 3605 3613 3629 3637 3645 3663 3693 3701 3717 3715 3715 3715 3715 3715 3715 371	3590 3598 3606 3614 3622 3630 3633 3646 3654 3670 3710 3718 3734 3750 3758 3758 3758 3768 3774 3774 3778 3778 3778 3778 3778	3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3679 3895 3703 3711 3719 3725 3743 3751 3759 3767 3775 3783 3791 3799 3807	7410 7420 7430 7440 7450 7460 7470 7500 7510 7520 7530 7660 7670 7670 7770 7770 77720 7730 7740	3840 3848 3856 3864 3872 3880 3912 3920 3928 3936 3944 3952 3960 3968 3976 4000 4016 4024 4032 4040 4048 4054 4054	3841 3849 3857 3865 3873 3881 3993 3913 3921 3923 3953 3953 3969 3969 4017 4009 4017 4025 4033 4041 4049 4047 4049 4047	3842 3850 3858 3864 3890 3914 3922 3930 3954 3954 3970 3978 3986 4010 4010 4010 4014 4024 4050 4054 4054 4056	3843 3851 3859 3867 3875 3883 3891 3915 3923 3931 3953 3963 3971 4019 4019 4019 4027 4043 4051 4059 4067	3844 3852 3860 3868 3892 3900 3916 3924 3932 3940 3948 3956 4028 4028 4028 4028 4036 4044 4052 4060 4068	3845 3853 3861 3869 3877 3885 3893 3901 3917 3925 3933 3941 3949 3957 3965 4013 4021 4029 4037 4045 4053 4061	3846 3854 3862 3870 38986 39902 3918 3926 39342 3950 3958 3968 3974 3984 4022 4024 4024 4030 4038 4046 4054 4062 4070	3847 3855 3863 3873 3879 3987 3993 3993 3993 3943 3959 3967 3975 3983 3999 4007 4023 4031 4039 4047 4055 4063	to 7777	to 4095
7010 7020 7050 7060 7070 7100 71100 7120 7130 7140 7140 7120 7200 7210 7210 7220 7230 7240 7350 7330 7340 7350	3584 3592 3600 3608 3616 3624 3643 3656 3664 3668 3704 3712 3720 3728 3736 3744 3752 3766 3768 3768 3776 3784 3792 3800 3808 3808	3585 3593 3601 3609 3617 3625 3633 3641 3667 3673 3673 3705 3713 3721 3721 3721 3737 3745 3753 3761 3769 3777 3785 3793 3801 3801 3801	3586 3594 3602 3618 3626 3638 3642 3650 3674 3682 3706 3714 3722 3738 3746 3757 3778 3786 3770 3788 3794 3802 3818	3587 3595 3603 3611 3627 3635 3643 3651 3665 3675 3675 3675 3707 3715 3723 3731 3731 3745 3763 3771 3779 3787 3783 3795 3803 3813	3588 3496 3604 3620 3628 3636 3636 3644 3652 3660 3708 3718 3724 3748 3748 3772 3780 3788 3784 3784 3784 3784 3784 3784 3784	3589 3497 3605 3613 3621 3629 3637 3645 3663 3677 3783 3791 3779 3775 3773 3781 3781 3783 3797 3805 3873 3813 3821	3590 3598 3606 3614 3622 3630 3638 3646 3678 3678 3710 3710 3714 3750 3774 3750 3774 3782 3798 3806 3814 3814 3814 3818	3591 3599 3607 3615 3623 3631 3639 3647 3655 3673 3711 3719 3727 3735 3743 3751 3752 3767 3775 3783 3791 3797 3807 3815 3807 3815	7410 7420 7430 7440 7450 7460 7470 7500 7510 7520 7530 7660 7670 7700 7710 7720 7730 7740 7750	3840 3848 3856 3864 3972 3880 3912 3920 3928 3936 3942 3952 3960 3968 3976 4000 4016 4024 4032 4040 4044 4048 4056 4064 4072	3841 3849 3857 3865 3873 3881 3897 3905 3913 3921 3937 3945 3953 3961 3969 3977 4001 4001 4017 4025 4033 4041 4067 4065 4067	3842 3850 3858 3866 3874 3882 3890 3914 3922 3930 3938 3946 4092 4012 4014 4018 4026 4058 4068 4068	3843 3851 3859 3867 3875 3883 3891 3923 3939 3947 3975 3963 3971 3979 4003 4003 4019 4027 4043 4043 4059 4069 4069 4075	3844 3852 3860 3868 3876 3894 3916 3924 3940 3940 3940 3940 3940 3940 4044 4020 4028 4044 4052 4060 4064 4064 4064 4064 4064 4064 406	3845 3853 3861 3869 3877 3885 3893 3901 3917 3925 3933 3941 3949 3953 3965 3973 3981 3989 4005 4001 4029 4037 4045 4061 4061 4061 4067	3846 3854 3870 3870 3983 3998 3998 3998 4006 4014 4022 4030 4030 4044 4054 4064 4078	3847 3855 3863 3871 3887 3897 3903 3911 3919 3927 3943 3951 3959 3967 3975 3983 3991 4003 4004 4074 4075 4063 4074 4079	to 7777	to 4095
7010 7020 7050 7060 7070 7100 7110 7120 7130 7140 7150 7170 7200 7210 7210 7220 7230 7240 7250 7270 7300 7310 7320 7330 73340	3584 3592 3600 3616 3624 3652 3640 3652 3664 3652 3672 3688 3696 3704 3712 3720 3736 3744 3752 3760 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3763 3764 3764	3585 3593 3601 36019 3617 3625 3633 3641 3687 3681 3689 3793 3705 3713 3729 3745 3753 3761 3769 3777 3785 3793 3809	3586 3594 3602 3610 3626 3634 3650 3658 3666 3774 3778 3778 3778 3778 3778 3778 3778	3587 3595 3603 3611 3627 3635 3663 3661 3659 3663 3691 3707 3715 3763 3763 3763 3763 3771 3779 3787 3787 3787 3787 3787 3787 3883	3588 3496 3604 3612 3628 3636 3644 3692 3700 3712 3748 3748 3756 3764 3772 3780 3788 3798 3798	3589 3497 3605 3613 3629 3637 3645 3663 3693 3701 3717 3765 3773 37757 3	3590 3598 3606 3614 3622 3630 3633 3646 3654 3670 3710 3718 3734 3750 3758 3758 3758 3768 3774 3774 3778 3778 3778 3778 3778	3591 3599 3607 3615 3623 3631 3639 3647 3655 3663 3679 3895 3703 3711 3719 3725 3743 3751 3759 3767 3775 3783 3791 3799 3807	7410 7420 7430 7440 7450 7460 7470 7500 7510 7520 7530 7660 7670 7670 7770 7770 77720 7730 7740	3840 3848 3856 3864 3872 3880 3912 3920 3928 3936 3944 3952 3960 3968 3976 4000 4016 4024 4032 4040 4048 4054 4054	3841 3849 3857 3865 3873 3881 3993 3913 3921 3923 3953 3953 3969 3969 4017 4009 4017 4025 4033 4041 4049 4047 4049 4047	3842 3850 3858 3864 3890 3914 3922 3930 3954 3954 3970 3978 3986 4010 4010 4010 4014 4024 4050 4054 4054 4056	3843 3851 3859 3867 3875 3883 3891 3915 3923 3931 3953 3963 3971 4019 4019 4019 4027 4043 4051 4059 4067	3844 3852 3860 3868 3892 3900 3916 3924 3932 3940 3948 3956 4028 4028 4028 4028 4036 4044 4052 4060 4068	3845 3853 3861 3869 3877 3885 3893 3901 3917 3925 3933 3941 3949 3957 3965 4013 4021 4029 4037 4045 4053 4061	3846 3854 3862 3870 38986 39902 3918 3926 39342 3950 3958 3968 3974 3984 4022 4024 4024 4030 4038 4046 4054 4062 4070	3847 3855 3863 3873 3879 3987 3993 3993 3993 3943 3959 3967 3975 3983 3999 4007 4023 4031 4039 4047 4055 4063	to 7777	to 4095

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
						.303	.380859
.003	.005859	.103	.130859	.203	.255859		
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.007		1					
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	396484
	.023437					.314	
.014		.114	148437	.214	.273437		.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
000	040075	100	474075	200	200075	220	424075
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	137	.185546	.237	.310546	.337	.435546
		1.00	407500		040500		407500
.040	.062500	.140	.187500	.240	.312500	.340	437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	212890	.255	.337890	.355	462890
056	.089843	.156	214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
060	002750	160	210750	260	242750	360	460750
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	226562	.264	.351562	.364	.476562
.065		165		.265		.365	
000	.103515		.228515	200	.353515	000	.478515
.066	.105468	.166	.230468	266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
070	100275	170	224275	270	250275	270	101275
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	365234	.373	.490234
.074	.117187	.174	.242187	.274	367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
076	.121093	.176	.246093	.276	.371093	.376	.496093
.076 .077	.123046	.177	248046	.277	373046	.0,0	.498046

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000732
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000007	.000020	.000107	.000270	.000207	.000314	.000307	.000753
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
	.000049						
.000015		.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000020	.000064	.000120	.000303				
				.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	000226	.000572	.000326	000816
.000027	.000087	.000127	.000320	.000227	.000576	.000327	.000820
000000	000004				000570		
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	000233	.000591	.000333	.000835
.000034	.000106	.000133	.000350	000233	.000595	.000334	.000839
.000034	.000100	.000134	.000354				
				.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000041	.000129	.000141	.000370	.000241	.000617	.000341	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
000050	000153	000150	000300	000050	000640	000050	000005
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000177	.000156	.000413	.000256	.000663	.000356	.000907
.000057	.000175	.000156	.000419	.000256	.000667	.000356	.000907
							.000311
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000162	.000434	.000262	.000673	.000362	.000923
.000064	.000198	.000164	.000442	000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000070	.000213	.000170	.000461		.000701		
				.000271		.000371	.000949
.000072	.000221	.000172	000465	.000272	000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	000957
.000073	.000228	.000174	.000473	.000274	.000717	.000374	.000961
					.000720		
.000074	000232	000175	000476	1 (1011775			
.000074 .000075	.000232	.000175	.000476	.000275		.000375	.000965
.000074	.000232 .000236 .000240	.000175 .000176 .000177	.000476	.000275	.000724	.000375	.000968

OCTAL-DECIMAL FRACTION CONVERSION TABLE

						I	
OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000410	.001010	.000510	.001251	.000611	.001499	.000710	.001733
.000411	.001014	.000511	.001258	.000611	.001502	.000711	.001743
.000413	.001018	.000512	.001262	.000612	.001506	.000712	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
000400	001007	000500					
.000420 .000421	.001037 .001041	.000520 .000521	.001281 .001285	.000620 .000621	.001525 .001529	.000720	.001770
.000421	.001041	.000521		.000621		.000721 -	.001773
.000422	.001045	.000522	.001289 .001293	.000622	.001533 .001537	.000722	.001777 .001781
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000426	.001060	.000525	.001304	.000625	.001544	.000725	.001789
.000428	.001064	.000526	.001304	.000626	.001548	.000726	.001792
.000430	.001068 .001071	.000530	.001312	.000630	.001556	.000730	.001800
.000431		.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571 .001575	.000734	.001815
.000435	.001087	.000535	.001331	.000635		.000735	.001819
.000436 .000437	.001091 .001094	.000536 .000537	.001335 .001338	.000636	.001579 .001583	.000736 .000737	.001823 .001827
.000437	.001094	.000537	.001336	.000637	.001563	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000761	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001413	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001441	.000671	.001682	.000771	.001926
.000472	.001201	.000572	.001441	.000672	.001689	.000772	.001930
.000473	.001201	.000574	.001445	.000673	.001689	.000773	.001934
.000474	.001209	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001213	.000576	.001453	.000676	.001701	.000775	.001941
.000470	.001213	.000578	.001461	.000676	.001701	.000776	.001945
.000477	.501210	.000577	.501401	.000677	.001705	.000777	.001949

GLOSSARY

GLOSSARY OF TeleProgramming TERMS

The following glossary gives the meaning of terms that are used in a relatively specialized sense in this manual.

ADDER

In general, a device used to add two quantities. Specifically, the borrow structure in the subject computer.

ADDRESS

The number designating a storage location; also the storage location itself.

NO ADDRESS MODE The TeleProgrammer permits the performance of arithmetic and logical operations by an 8-bit constant associated with the instruction and using the memory location immediately following the instruction as an 8-bit operand.

MEMORY ADDRESS MODE A mode of addressing wherein an 8-bit operand in any storage location is addressed by the memory location (immediately following the instruction) and the contents of the Tag register as referenced by T.

INDIRECT ADDRESS MODE Instructions employing indirect addressing use the memory location immediately following the instruction to refer to one of the first 256 storage locations. The contents of this address are used along with the contents of the Tag register as the address of the operand.

BIT Binary digit; may be either "1" or "0".

BORROW In a subtractive counter or accumulator, a signal

indicating that in stage n, a "1" was subtracted

from a "0".

BUFFER Noun: A device in which data are stored tem-

porarily in the course of transmission from one point to another. Verb: To store data temporarily.

BUFFERED INPUT/OUTPUT

A term indicating that the computer may carry on high speed computation at the same time it is exchanging data with a peripheral device. In the TeleProgrammer, this term must be distinguished from normal I/O, during which the computer cannot engage in computation.

CARRY

In an additive counter or accumulator, a signal indicating that in stage n, a "1" was added to a "1".

CHANNEL

A transmission path that connects the computer to a given external equipment.

CLEAR

A command that removes a quantity from a register by placing every stage in the "0" state.

COMMAND

A signal that performs a unit operation, such as transmitting contents of one register to another, shifting a register, setting a flip-flop.

COMPLEMENT

Noun: See One's Complement to Two's Complement. Verb: A command which produces the one's complement of a given quantity.

CONTENT

The quantity or word held in a register or storage location.

CORE

A small ferromagnetic toroid used as the bistable device for storing a bit in a memory plane.

COUNTER

A register with provisions for increasing or decreasing its content by 1 upon receiving the appropriate command.

END-AROUND BORROW A borrow that is generated in the highest order of an accumulator or counter, and is sent directly to the lowest order stage.

ENTER

To manually place in a register a quantity that is not from storage. In the TeleProgrammer, quantities may be entered in only the Tag A, P, and Z registers.

FUNCTION CODE

The lower 3 quartics of the first word in the instruction set.

INPUT DISCONNECT During an input instruction, a signal sent to the computer by the external device to indicate that the device has completed all available transmissions to the computer.

INPUT REQUEST

A request, by the computer, for information from an external device. Occurs during input instruction only. (See Resume.)

INTERRUPT

A signal (or class thereof) which, when received and recognized by the computer, forces the computer to forestall its current operation and jump to a subroutine, the starting address of which is determined by the class of the interrupt. A subroutine may have any number of options. It may merely stop the computer, it may determine the nature of the interrupt in order to take corrective measures, or it may return the computer to another phase of the main program.

JUMP

An instruction that jumps from one sequence of instructions to a second, and makes no preparation for returning to the first sequence.

LOAD

To place a quantity from storage in the A register.

LOCKOUT

Any function (usually of machine logic) that inhibits an action which would normally occur were the lockout not imposed.

LOGICAL PRODUCT In Boolean algebra, the AND function of several terms. The product is "1" only when all the terms are "1"; otherwise it is "0". Sometimes referred to as the result of "bit-by-bit" multiplication.

LOGICAL SUM

In Boolean algebra, the OR function of several terms. The sum is "1" when any or all of the terms are "1"; it is "0" only when all are "0".

MASK

In the information of the logical products of two quantities, one of them may be used as a mask for the other. The mask determines what part of the other quantity is to be considered. Wherever the mask is "0", that part of the other quantity is cleared, but wherever the mask is a "1", the other quantity is left unaltered.

MASTER CLEAR (MC)

A general command produced by placing the Load/Clear switch in the down (CLEAR) position. An MC clears all of the crucial registers and control FFs to prepare for a new mode of operation.

MODULUS

An integer which describes certain arithmetic characteristics of registers, especially counters and accumulators, within a digital computer. The modulus of a device is defined by rn for an open ended device and rn-1 for a closed (end-around) device, where r is the base of the number system used and n is the number of digit positions (stages) in the device. Generally, devices with modulus rn use two's complement arithmetic procedures, and devices with modulus rn-1 use one's complement procedures.

ONE'S

COMPLEMENT With reference to a binary number, that number

which results from subtracting each bit of the given number from the bit "1". A negative number is expressed by the one's complement

of the corresponding positive number.

OPERAND The quantity specified by the 4 quartic digits of

the second word of the instruction set. This quantity is operated upon in the execution of the

instruction.

OPERATION CODE The lower 3 quartics of the first word in the

instruction set also called Function Code and identified by the letter, F. After the code is translated, it conditions the computer for execu-

tion of the specified instruction.

OVERFLOW The condition in which the capacity of a register

is exceeded.

PARTIAL ADD An addition without carries. Accomplished by

toggling each bit of the augend where the corre-

sponding bit of addend is a "1".

PROGRAM A precise sequence of instructions that accom-

plishes a computer routine; a plan for the solution

of a problem.

QUARTIC A number system with a base of four. These

numbers are normally partitioned into groups of

two for ease of reading.

READ To place a quantity from a storage location into

a register. The quantity in storage remains

unchanged.

READY The input/output control signal sent by either the

computer or an external equipment to alert the device that is to receive a transmission. The ready signal indicates that the word or character

has been transmitted.

RELATIVE A mode of addressing wherein the address of ADDRESSING the operand is determined by adding (or subtract-

ing) the contents of the execution address portion of the instruction word to (or from) the instruction

address.

REPLACE In the title of an instruction, the result of the

execution of the instruction is stored in the location from which the initial operand was obtained.

RESUME The output control signal sent by an external

equipment to indicate that it is prepared to receive another word or character. The resume signal is thus a request for data. (See Input Request.)

ROUTINE The sequence of operations which the computer

performs under the direction of a program.

SHIFT To move the bits of a quantity right or left.

SIGN BIT The bit in the highest-order stage of the register

(in registers where a quantity is treated as signed by use of one's complement notation). If the bit is "1", the quantity is negative; if the

bit is "0", the quantity is positive.

SIGN EXTENSION The duplication of the sign bit in the highest-order

stages of a register.

STATUS

- 1) The condition of an external device, as reflected in the response given to a status request interrogation by the computer.
- 2) The condition of the computer as shown by the Status Mode indicator on the console. May variously indicate what it is presently doing, why it stopped, or what it will do when it next starts.

TRANSMISSION FORCED

A transmission where both set and clear inputs, only one of which will be a "1", are simultaneously gated into a FF which has not been cleared previously.

TRANSLATION

An indication of the content of a group of bit registers. A complete translation gives the exact content, while a partial translation indicates only that the content is within certain limits.

TWO's COMPLEMENT

That number which results from subtracting each bit of a number from "0". The two's complement may be formed by complementing each bit of the given number and then adding one to the result, performing the required carries.

WORD

A unit of information which has been coded for use in the computer as a series of bits. The normal word length is 8 bits.

WRITE

To enter a quantity into a storage location.